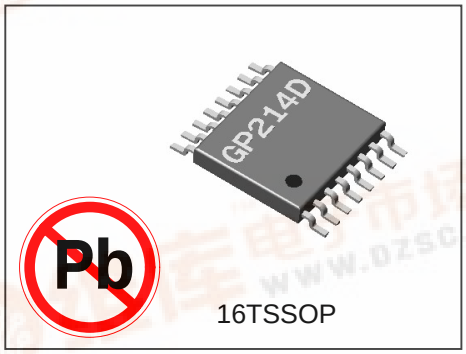
DESCRIPTION

The GP214D is a dual frequency synthesizer designed for RF operation up to 1.4GHz. The device contains prescalers, programmable reference, and feedback frequency dividers, phase detectors, and charge pumps necessary for the precision control of dual VCO loops. Data transfer is made via a simple serial data interface. The GP214D is fabricated using advanced CMOS process and available in a 16-pin TSSOP plastic package with 0.65mm pitch.

FEATURES

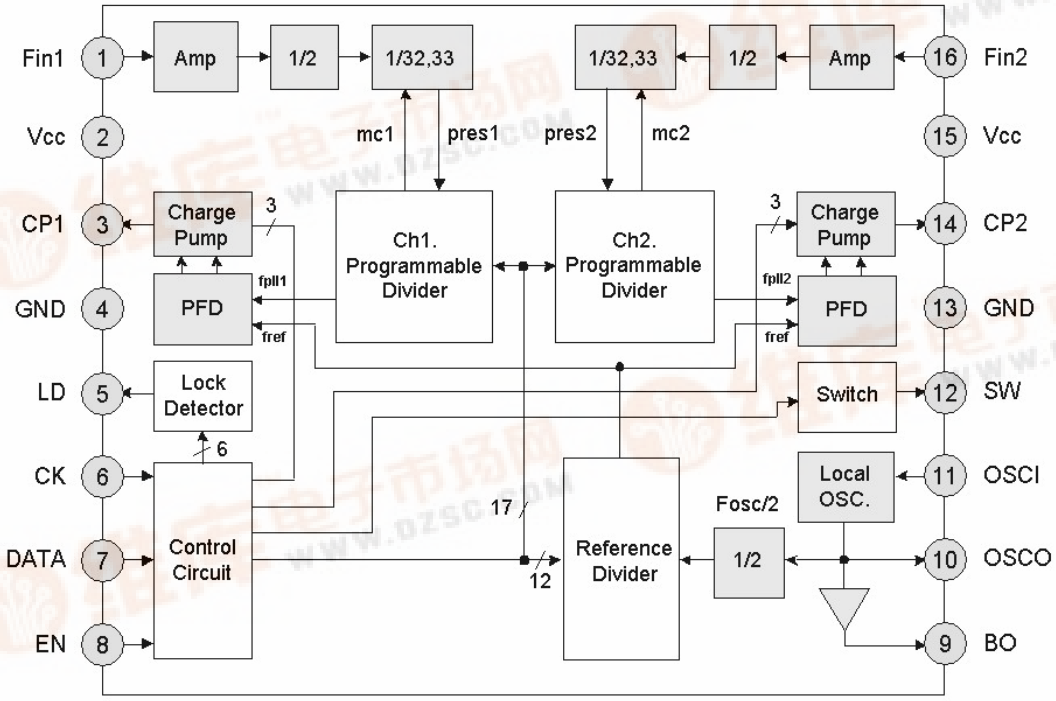
- Two systems for transmitter and receiver
- 2.4V to 5.0V operation (100MHz to 1.4GHz)
- Low current consumption
  8.5mA @ 3.0V (Typ.)
- Modulus prescaler, 64 / 66
- Selectable charge pump current
  ± 0.2mA, ± 0.4mA, ± 0.8mA, ± 1.6mA



APPLICATIONS

- Portable wireless communications (PCS, cordless)
- Other wireless communication systems

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function Description		I / O
1	Fin1	RF input, channel 1.		I
2, 15	Vcc	Power supply. Two pins are connected each other.		-
3	CP1	Charge pump output, channel 1. Charge pump current is selected by the input serial data.		O
4, 13	GND	Ground. Two pins are connected.		-
5	LD	Output of lock detection. It is the open drain output.		O
6	CK	Clock input.	Serial data interface.	I
7	DATA	Serial data input.		
8	EN	Input of enable signal.		
9	BO	Output of buffer amplifier. The local signal passes through the buffer amplifier.		O
10	OSCO	Oscillator output.		O
11	OSCI	PLL reference input. Typically connected to a TCXO output.		I
12	SW	Switchover terminal to control time constant of loop filter. It is the open drain output. When switched off, it's normal output.		O
14	CP2	Charge pump output, channel 2.		O
16	Fin2	RF input, channel 2.		I

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Power supply voltage	Vcc	5.5	V
Operating temperature	T_{OPR}	-30 to +85	°C
Storage temperature	T_{STG}	-35 to +150	°C
ESD (Human body model)		2000	V

Note: This device is ESD sensitive. Appropriate ESD protection is required for device handling and assembly.

ELECTRICAL CHARACTERISTICS

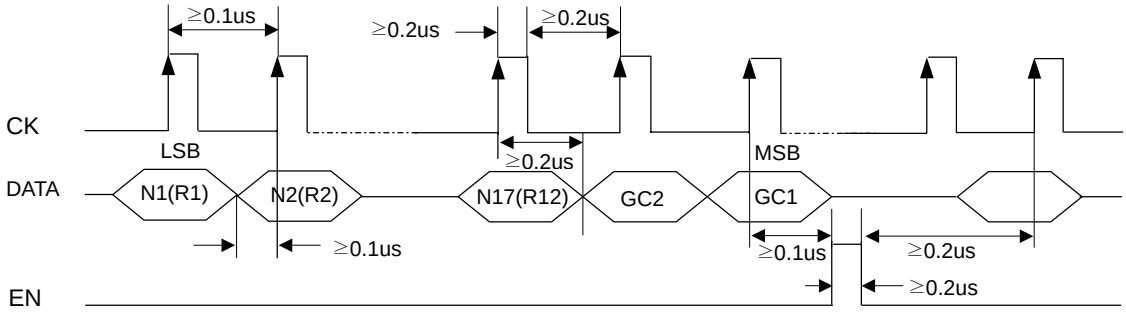
(Unless otherwise specified, Vcc = 3.0V, Ta = 25°C)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Operating power supply voltage	Vcc	Fin1= Fin2= 200MHz~1.4GHz		2.4	3.0	5.0	V
Operating current consumption	Icc	Fin1= Fin2= 800MHz/ -5dBm input		7.0	8.5	14.5	mA
Standby current	I_{SB}	Standby mode		-	0	80	µA
Fin operating frequency	Fin	Fin1=Fin2= -5dBm		200	-	1400	MHz
Fin input sensitivity	Fin	Fin1= Fin2= 200~1200MHz	Vcc = 2.4V	-15	-	10	dBm
			Vcc = 3.0V	-15	-	10	
			Vcc = 5.0V	-15	-	10	
		Fin1= Fin2= 1200~1400MHz	Vcc = 2.4V	-15	-	0	
			Vcc = 3.0V	-15	-	0	
			Vcc = 5.0V	-15	-	0	
OSCI operating frequency	F_{OSC}	V_{Fin}= 0dBm, sinewave		4	-	40	MHz
OSCI input voltage	V_{OSC}	F_{OSC}= 4~10MHz	Vcc= 2.4~3.7V	-10	0	10	dBm
		F_{OSC}= 10~40MHz	Vcc= 2.4~5.0V	-15	0	20	
Serial data input high voltage (CK, DATA, EN)	V_{IH}	Vcc= 1.7 to 5.0V		Vcc – 0.2	Vcc	-	V
Serial data input low voltage (CK, DATA, EN)	V_{IL}	Vcc= 1.7 to 5.0V		-	0	0.2	V
Charge pump output current	I_{CP1}	CP1= 0, CP2= 0 (V_{CP}= 1/2 Vcc)		- 15%	± 1.6	+ 15%	mA
	I_{CP2}	CP1= 1, CP2= 0 (V_{CP}= 1/2 Vcc)		- 15%	± 0.2	+ 15%	
	I_{CP3}	CP1= 0, CP2= 1 (V_{CP}= 1/2 Vcc)		- 15%	± 0.4	+15%	
	I_{CP4}	CP1= 1, CP2= 1 (V_{CP}= 1/2 Vcc)		- 15%	± 0.8	+15%	
Charge pump leakage	I_{CPL}	Standby mode (V_{CP}= 1/2 Vcc)		-1	-	1	µA

PROGRAMMING DESCRIPTION

SERIAL DATA INPUT AND TIMING

The programmable functions are accessed through the MCU serial data interface. The interface includes clock (CK, pin 6), data (DATA, pin 7) and enable signal (EN, pin 8). Serial data controls programmable reference counter and programmable counters in channel 1 and channel 2. The serial data is clocked in on the rising edge of clock and transferred into the shift register composed of 17-bit data field and 2-bit control field. When EN is high, stored data is latched. Data is entered LSB first.



GROUP CODE AND LOCATION

The data stored in the shift register is loaded into one of four appropriate latches depending on the state of group code (control bits) listed below.

Control Bits		Data Location
GC2(MSB-1)	GC1(MSB)	
0	0	Control Latch
1	0	Ch 1 N Latch
0	1	Ch 2 N Latch
1	1	OSC R Latch

OPTIONAL CONTROL

The control register enables various functions shown in the table below.

LSB		Channel 1			Channel 2								MSB
Bit1	**Bit2**	**Bit3**	**Bit4**	**Bit5**	**Bit6**	**Bit7**	**Bit8**	**Bit9**	**Bit10**	**Bit11**	**Bit12**	**Bit13**	**Bit14**
T	**CP**	**CP1**	**CP2**	**SB1**	**CP1**	**CP2**	**SB2**	**SBR**	**LD1**	**LD2**	**SW**	**GC2**	**GC1**
Test Mode	Charge Pump Polarity	Charge Pump Output Current		Ch 1 Standby	Charge Pump Output Current		Ch2 Standby	Ref. Divider Standby	Lock Detector		Filter Switch	Group Code “0”, “0”	

- Test mode selection (T)

H: test mode, L: normal mode

- Output polarity of charge pump (CP)

CP is set to “0” at normal and changed to “1” when reverse operation, according to the dependence of VCO output frequency upon VCO input voltage. “Normal” denotes proportional response in the frequency to the VCO input voltage.

- Charge pump output current (CP1 and CP2)

Charge pump employs circuits characterized by constant output current. The output current can be selected for the best performance.

Control Bits		Charge Pump Output Current
CP1	**CP2**	
0	0	±1600μA
0	1	±200μA
1	0	±400μA
1	1	±800μA

- Test mode and lock detector output (T, LD1 and LD2)

The LD state can be changed via controlling SB1, SB2, LD1 and LD2.

T	SB1	SB2	LD1	LD2	LD Output State
0	0	0	0	0	low
			0	1	channel2
			1	0	channel1
			1	1	channel 1 and channel2
		1	0	0	low
			0	1	high
			1	0	channel1
			1	1	channel1
	1	0	0	0	low
			0	1	channel2
			1	0	high
			1	1	channel2
		1	0	0	low
			0	1	high
			1	0	high
			1	1	high
1	1	0	0	0	low
			0	1	pres2
			1	0	fpll2
			1	1	fref
	0	1	0	0	div4
			0	1	pres1
			1	0	fpll1
			1	1	fosc/2
	1	1	×	×	low
	0	0	×	×	low

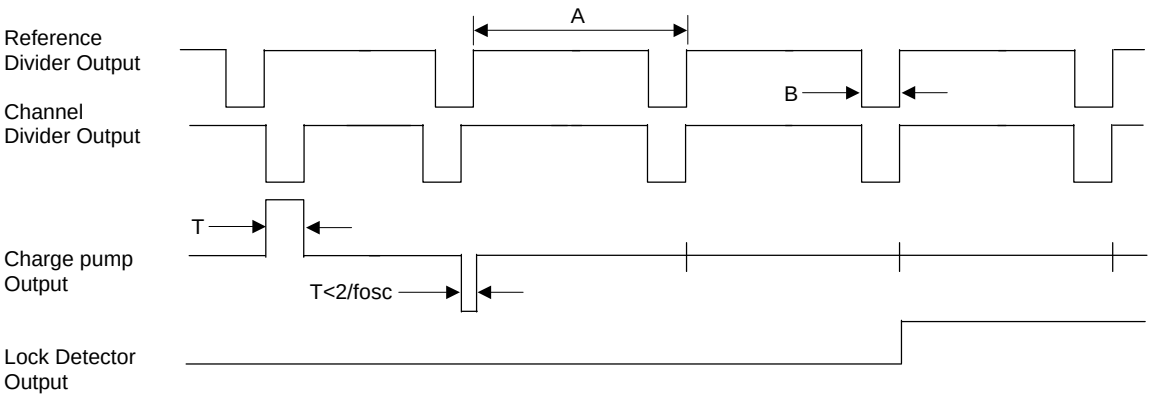
▪ Lock detector output

When the phase difference is detected, LD (pin 5) goes “L”. When locked or at standby, LD changes to H”. In case where the time difference, “T” less than 2/fosc (T<2/fosc) continues for more than three cycles of reference counter output, LD goes “H”.

Fosc: OSCI operating frequency (LOCAL OSC)
T: time difference of the pulse between reference divider output and channel divider output

$$A = \frac{\text{Number of divisions by reference dividers}}{\text{fosc}}$$

$$B = \frac{2}{\text{fosc}}$$



▪ Programmable standby mode (SB1, SB2 and SBR)

Standby mode is controlled by three control bits of SB1, SB2 and SBR. The standby control of channel 1 and channel 2 can be made by SB1 and SB2. The on/off of reference divider is controlled by SBR.

Control Bit			Standby Mode Status			
SB1	**SB2**	**SBR**	**CH1**	**CH2**	**REF**	**Mode Status**
0	0	0	ON	ON	ON	Inter-locking
0	1	0	ON	OFF	ON	CH1 locking
1	0	0	OFF	ON	ON	CH2 locking
1	1	0	OFF	OFF	ON	REF ON
1	1	1	OFF	OFF	OFF	Standby

- Filter switch control (SW)

SW terminal, for switching time constant of loop filter is controlled by "SW" bit. High lock mode and normal lock mode can be arbitrarily selected by filter switch control (SW) with the charge pump output current.

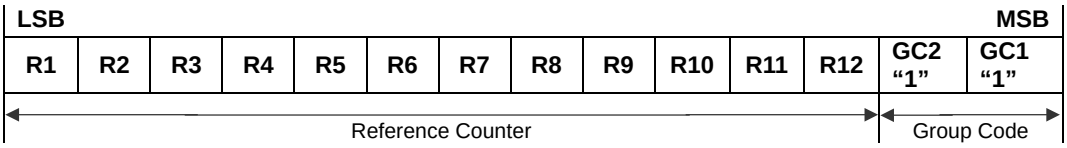
Control Bits			Mode
SW	CP1	CP2	
0	0	0	High Lock
0	0	1	
0	1	0	
0	1	1	
1	0	0	Normal Lock
1	0	1	
1	1	0	
1	1	1	

CRYSTAL OSCILLATOR CIRCUIT (OSCI, OSCO) AND BUFFER OUT (BO)

Reference frequency input is made directly to OSCI (pin 11). Buffer output (BO, pin 9) can be used for the 2nd mixer input.

REFERENCE COUNTER

When the control bits (GC1, GC2) are "11", data is transferred from shift register into the OSC R latch which sets the divide ratio of 12-bit reference counter. The divide ratio is programmed using the bits as shown in the table below.

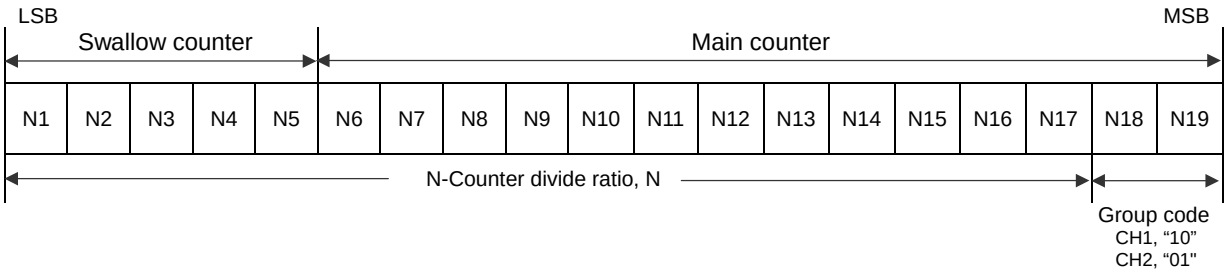


Divide ratio: 2×R = 2×(3 to 4095) = 6 to 8190

Divide Ratio	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

PROGRAMMABLE N-COUNTER, CH1 AND CH2

These counters consist of the 5-bit swallow counter, the 12-bit programmable main counter, and two modulus prescaler providing divisions of 64 and 66. The swallow counter and main counter enable to set any of 192 to 262142 divisions.



5-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

Divide ratio: 0 to 31, B≥A

Divide Ratio (A)	N5	N4	N3	N2	N1
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

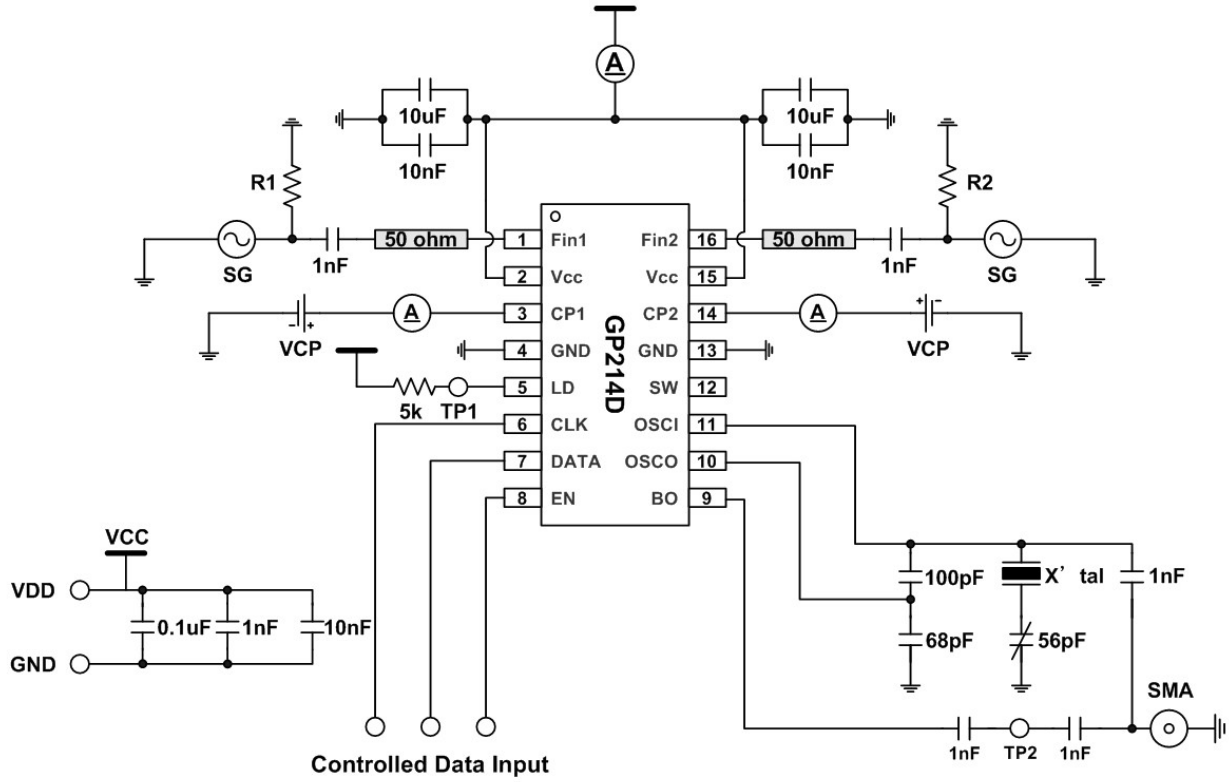
12-BIT MAIN COUNTER DIVIDE RATIO (B COUNTER)

Divide ratio: 3 to 4095

Divide Ratio (B)	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Divide ratio of channel 1 and 2 = N
N = 2×(32×B+A), B≥A
Divide ratio: 192 to 262142

TEST CIRCUIT



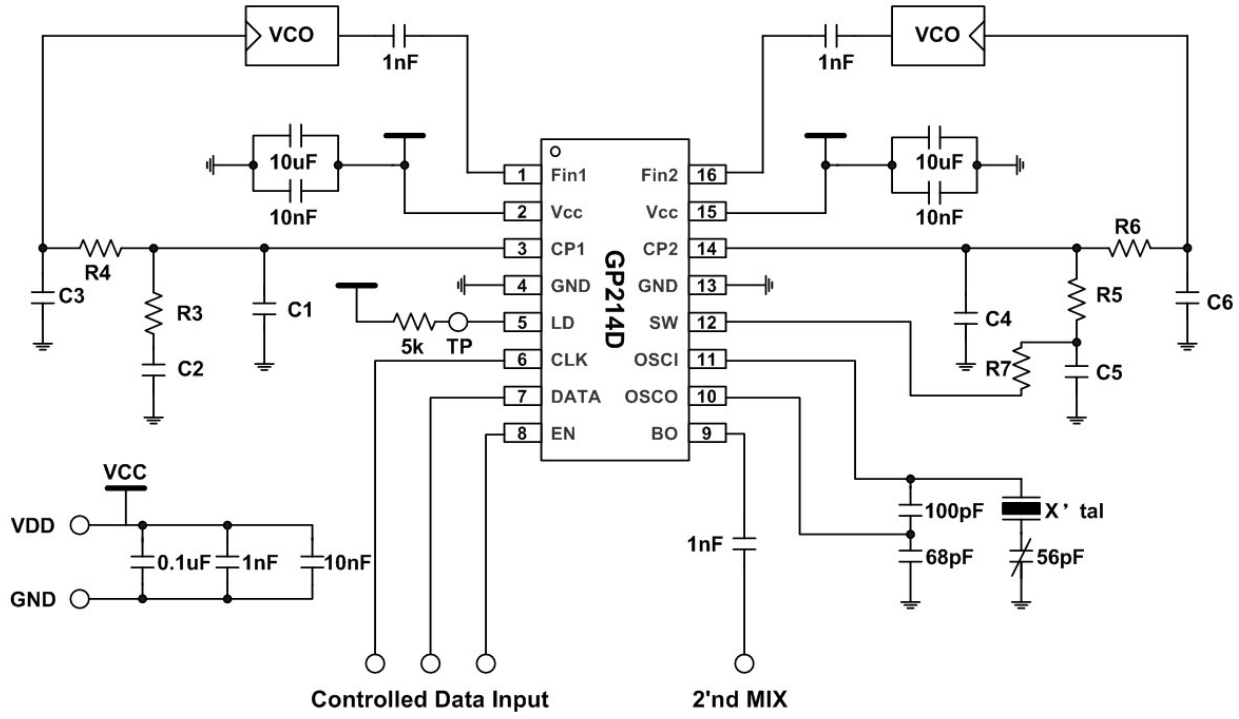
▪ Sensitivity measurement

- RF signal input is to be matched to 50Ohm and short line is recommended.
- R1 and R2 (51Ohm) are connected to GND.
- Tests at different bias and power levels are normally conducted.
- Turn on DC voltage and RF signal before the data programming.
- Frequency is monitored from TP1 (test point, 1) via frequency counter or oscilloscope.

▪ Charge pump current measurement

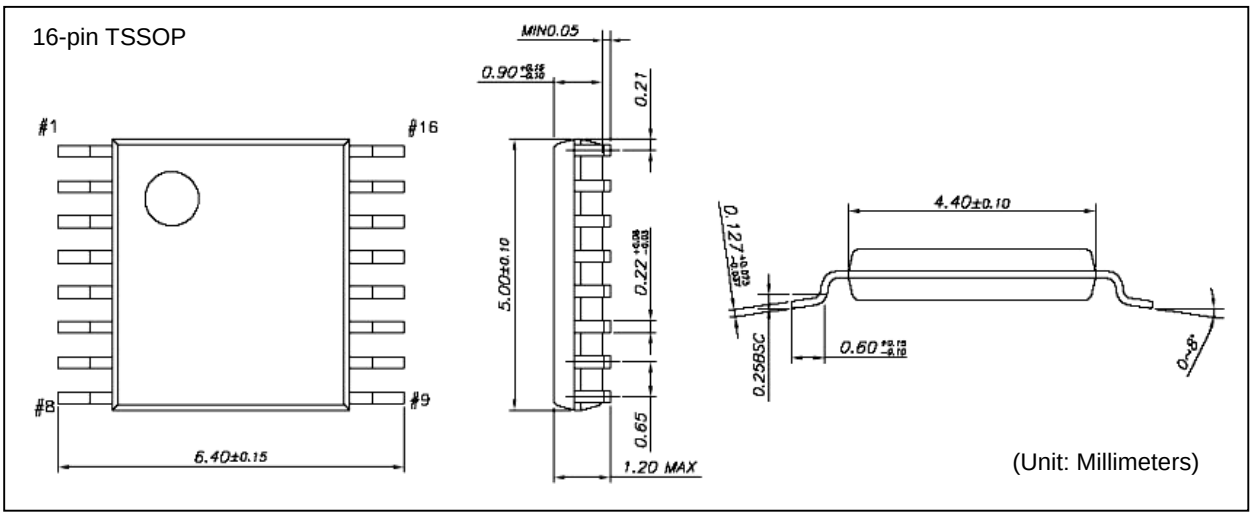
- VCP can be fixed to 1/2 VCC or varied from 0 to maximum VCC.
- Charge pump polarity is changed from normal to reverse.

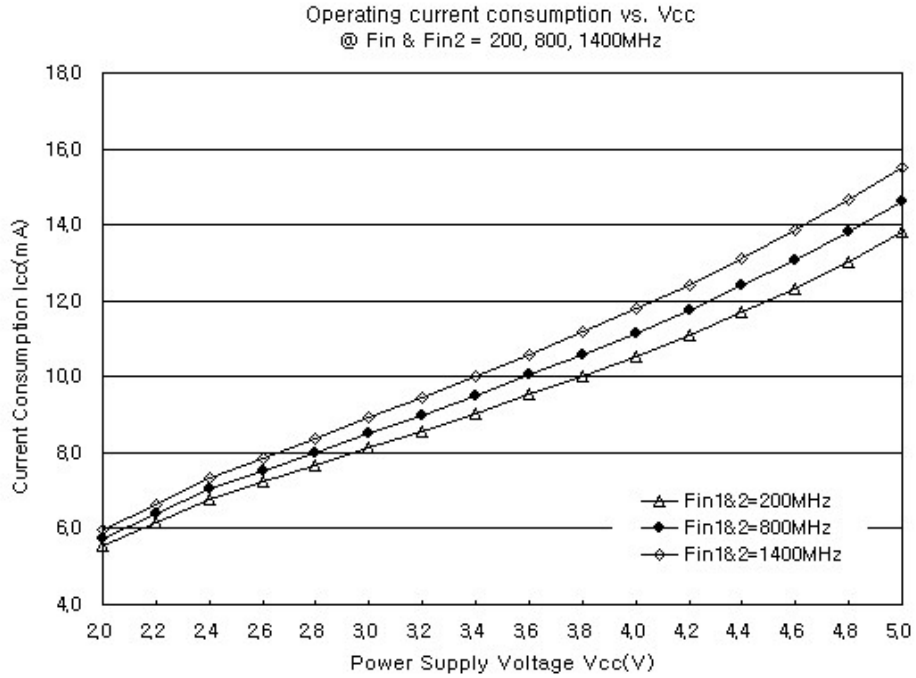
APPLICATION CIRCUIT

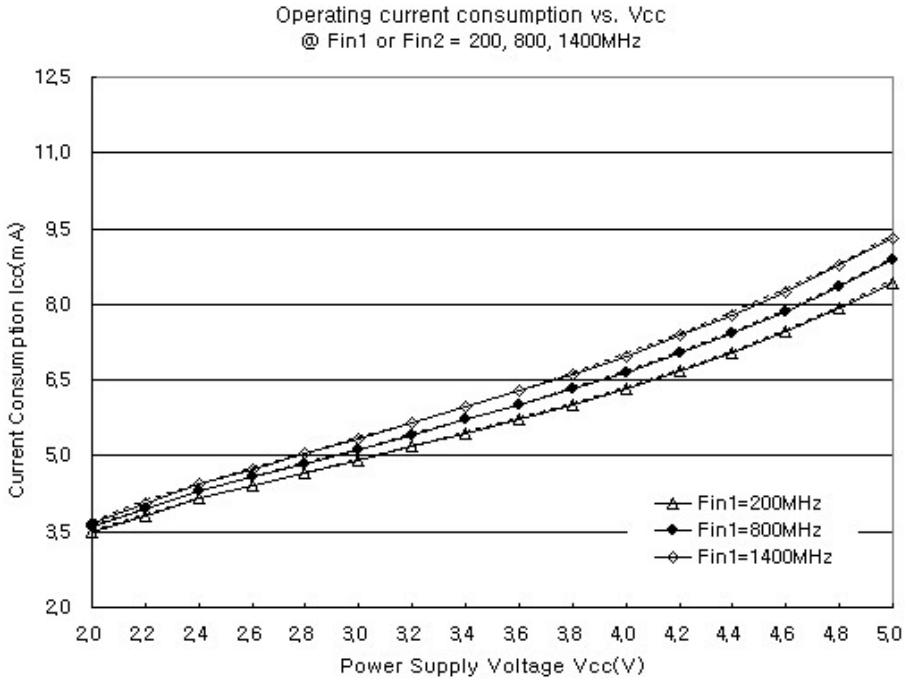


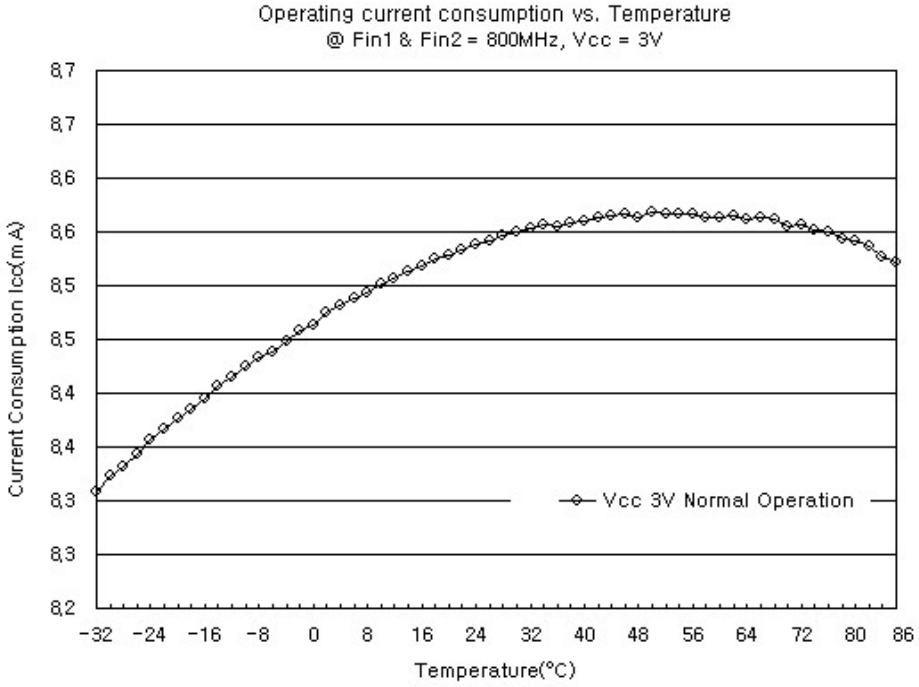
- R3~R6 & C1~C6: Loop filter components (depending on frequency, phase noise and lock time)
- SW turns on when R7 is connected.

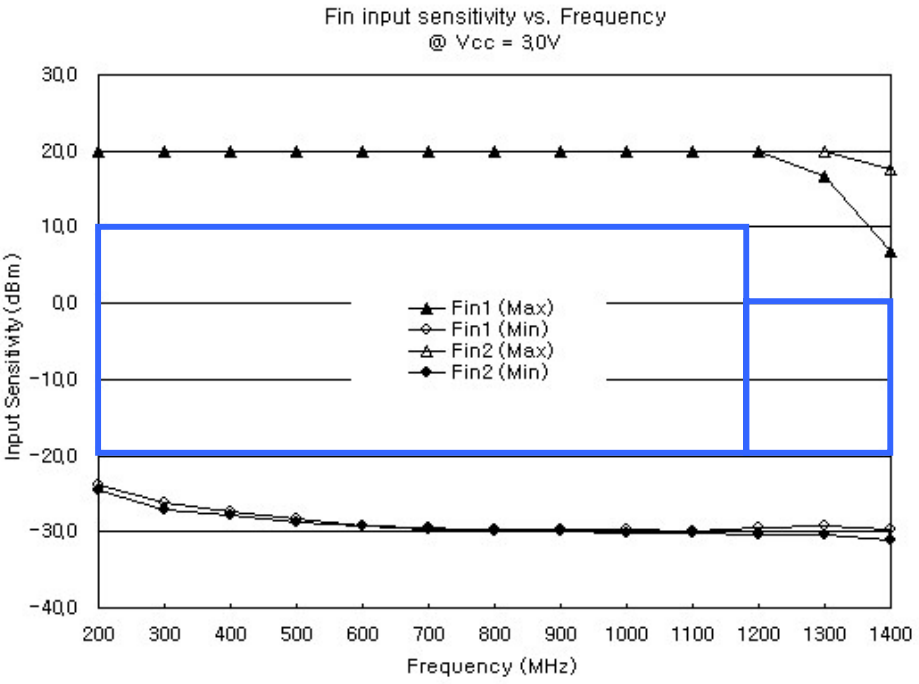
PACKAGE DEMENSIONS

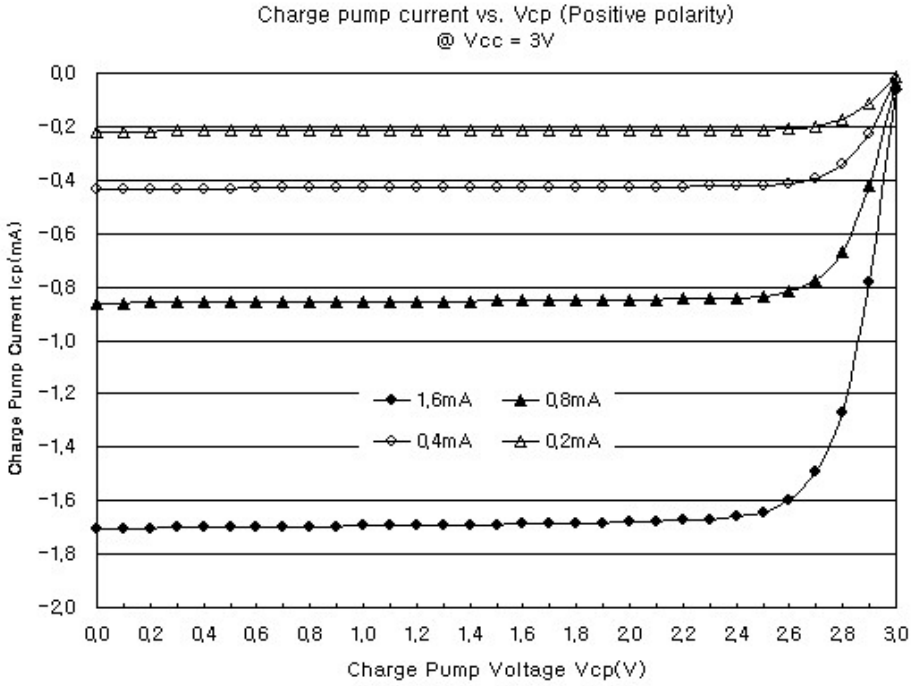


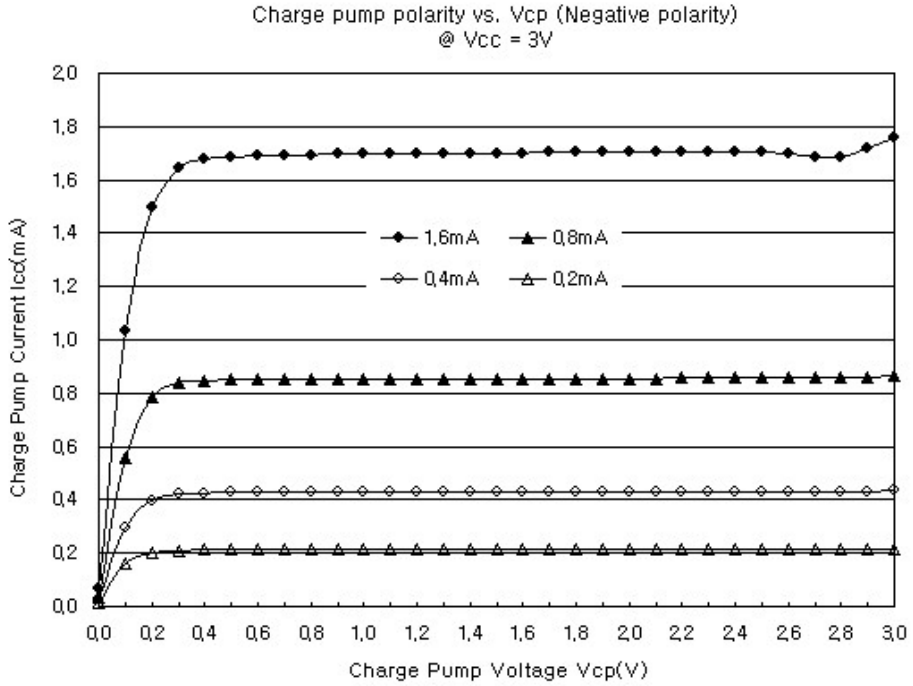

Operating current consumption vs. Vcc
@ Fin & Fin2 = 200, 800, 1400MHz
Current Consumption Icc(mA)
18,0
16,0
14,0
12,0
10,0
8,0
6,0
4,0
2,0 2,2 2,4 2,6 2,8 3,0 3,2 3,4 3,6 3,8 4,0 4,2 4,4 4,6 4,8 5,0
Power Supply Voltage Vcc(V)
Fin1&2=200MHz
Fin1&2=800MHz
Fin1&2=1400MHz

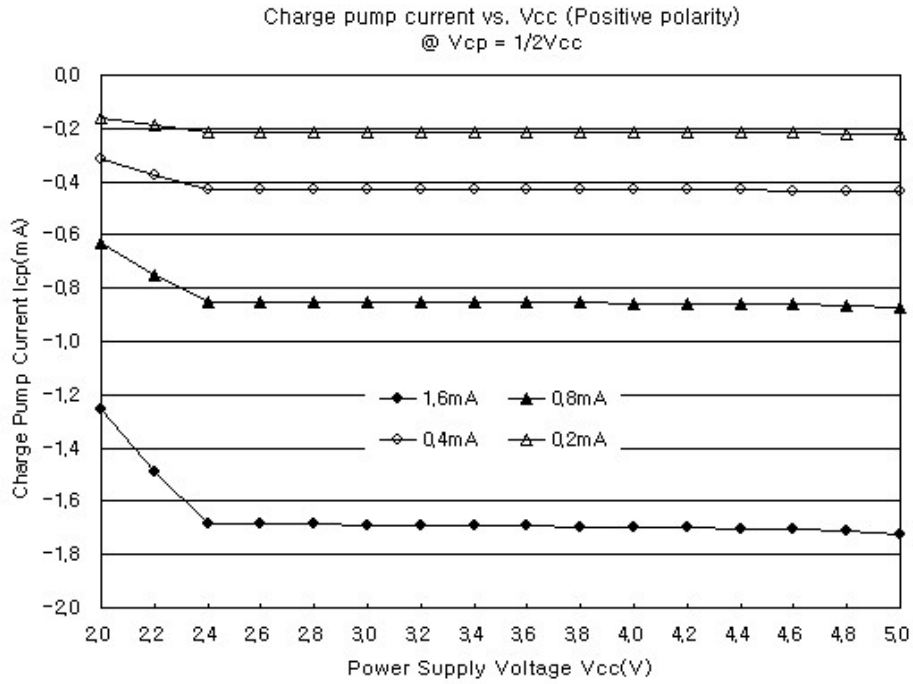

Operating current consumption vs. Vcc
@ Fin1 or Fin2 = 200, 800, 1400MHz
Current Consumption Icc(mA)
12,5
11,0
9,5
8,0
6,5
5,0
3,5
2,0
2,0 2,2 2,4 2,6 2,8 3,0 3,2 3,4 3,6 3,8 4,0 4,2 4,4 4,6 4,8 5,0
Power Supply Voltage Vcc(V)
Fin1=200MHz
Fin1=800MHz
Fin1=1400MHz

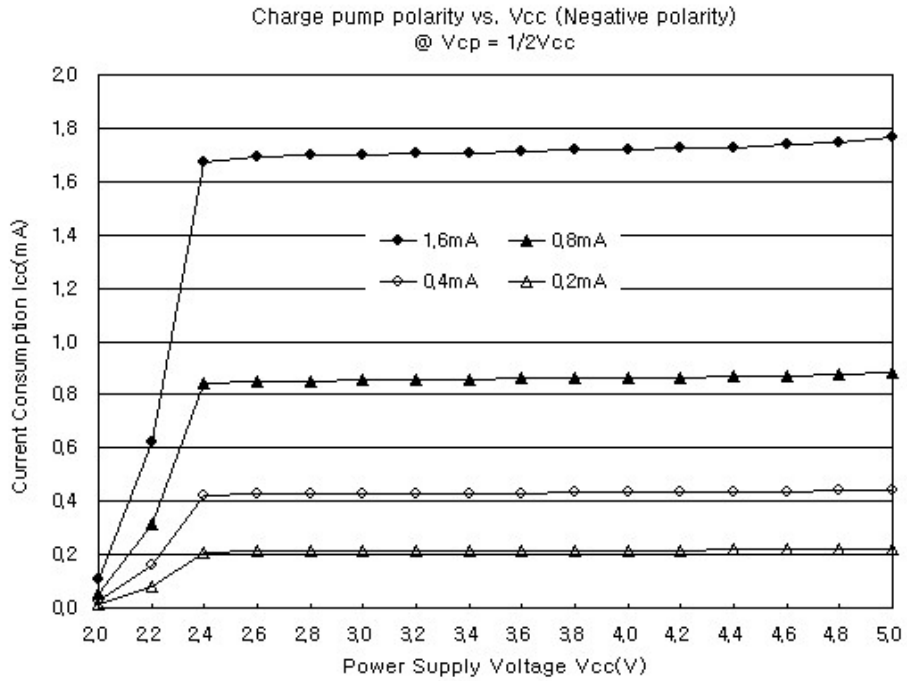

Operating current consumption vs. Temperature
@ Fin1 & Fin2 = 800MHz, Vcc = 3V
Current Consumption Icc(mA)
8.7
8.7
8.6
8.6
8.5
8.5
8.4
8.4
8.3
8.3
8.2
Vcc 3V Normal Operation
-32 -24 -16 -8 0 8 16 24 32 40 48 56 64 72 80 86
Temperature(°C)


Fin input sensitivity vs. Frequency
@ Vcc = 3.0V
Input Sensitivity (dBm)
30.0
20.0
10.0
0.0
-10.0
-20.0
-30.0
-40.0
Fin1 (Max)
Fin1 (Min)
Fin2 (Max)
Fin2 (Min)
200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400
Frequency (MHz)


Charge pump current vs. Vcp (Positive polarity)
@ Vcc = 3V
Charge Pump Current Icp(mA)
0,0
-0,2
-0,4
-0,6
-0,8
-1,0
-1,2
-1,4
-1,6
-1,8
-2,0
1,6mA
0,8mA
0,4mA
0,2mA
0,0 0,2 0,4 0,6 0,8 1,0 1,2 1,4 1,6 1,8 2,0 2,2 2,4 2,6 2,8 3,0
Charge Pump Voltage Vcp(V)


Charge pump polarity vs. Vcp (Negative polarity)
@ Vcc = 3V
Charge Pump Current Icp(mA)
2,0
1,8
1,6
1,4
1,2
1,0
0,8
0,6
0,4
0,2
0,0
1,6mA
0,8mA
0,4mA
0,2mA
0,0 0,2 0,4 0,6 0,8 1,0 1,2 1,4 1,6 1,8 2,0 2,2 2,4 2,6 2,8 3,0
Charge Pump Voltage Vcp(V)


Charge pump current vs. Vcc (Positive polarity)
@ Vcp = 1/2Vcc
Charge Pump Current Icp(mA)
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
-1.2
-1.4
-1.6
-1.8
-2.0
1.6mA
0.8mA
0.4mA
0.2mA
2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0
Power Supply Voltage Vcc(V)


Charge pump polarity vs. Vcc (Negative polarity)
@ Vcp = 1/2Vcc
Current Consumption Icc(mA)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
1.6mA
0.8mA
0.4mA
0.2mA
2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0
Power Supply Voltage Vcc(V)