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DM54LS273/DM74LS273 8-Bit Register with Clear

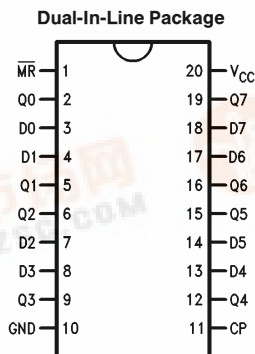
General Description

The 'LS273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

Features

- Edge-triggered
- 8-bit high speed register
- Parallel in and out
- Common clock and master reset

Connection Diagram



TL/F/9825-1

Order Number DM54LS273E, DM54LS273J,
DM54LS273W, DM74LS273M or DM74LS273N
See NS Package Number E20A, J20A, M20B,
N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0–D7	Data Inputs
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)
Q0–Q7	Flip-Flop Outputs



Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS273			DM74LS273			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW D _n to CP	15 15			15 15			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW D _n to CP	5 5			5 5			ns
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns
t _w (L)	$\overline{MR}$ Pulse Width LOW	20			20			ns
t _{rec}	Recovery Time $\overline{MR}$ to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −18 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	DM54	2.5		V
			DM74	2.7	3.4	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max, V _{IH} = Min	DM54		0.4	V
			DM74		0.35	
		I _{OL} = 4 mA, V _{CC} = Min	DM74		0.25	
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 7V V _I = 10V (DM54)			0.1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			−0.4	mA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	−20	−100	mA
			DM74	−20	−100	
I _{CC}	Supply Current	V _{CC} = Max			27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25^\circ C$

Symbol	Parameter	C _L = 15 pF				Units
		DM54LS		DM74LS		
				R _L = 2 kΩ		
		Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	30		30		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n		24 24		24 24	ns
t _{PLH}	Propagation Delay MR to Q _n		27		27	ns

Functional Description

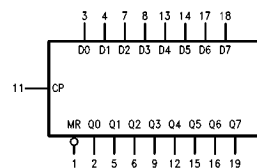
The 'LS273 is an 8-bit parallel register with a common Clock and common Master Reset. When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

Truth Table

MR	Inputs		Outputs Q_n
	CP	D_n	
L	X	X	L
H		H	H
H		L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

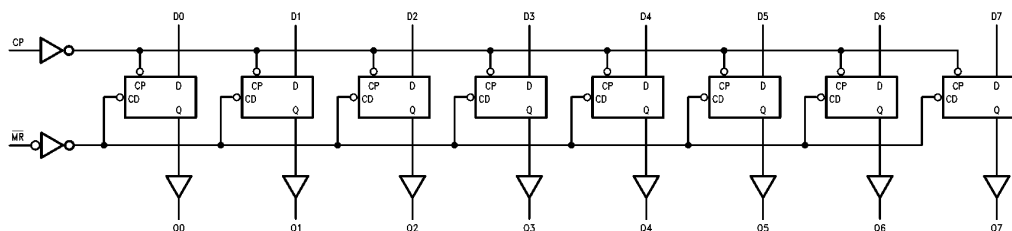
Logic Symbol



TL/F/9825-2

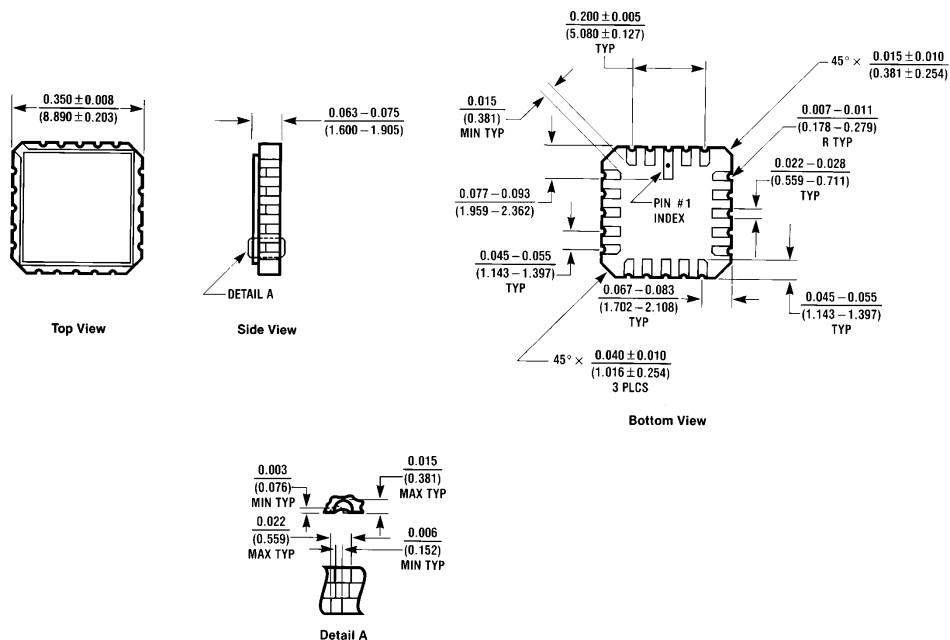
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram



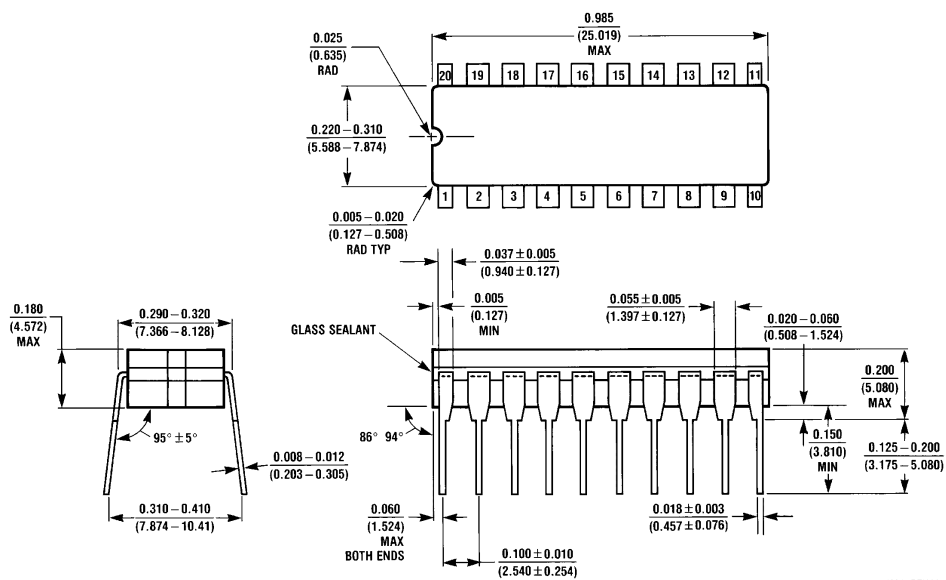
TL/F/9825-3

Physical Dimensions inches (millimeters)



E20A (REV D)

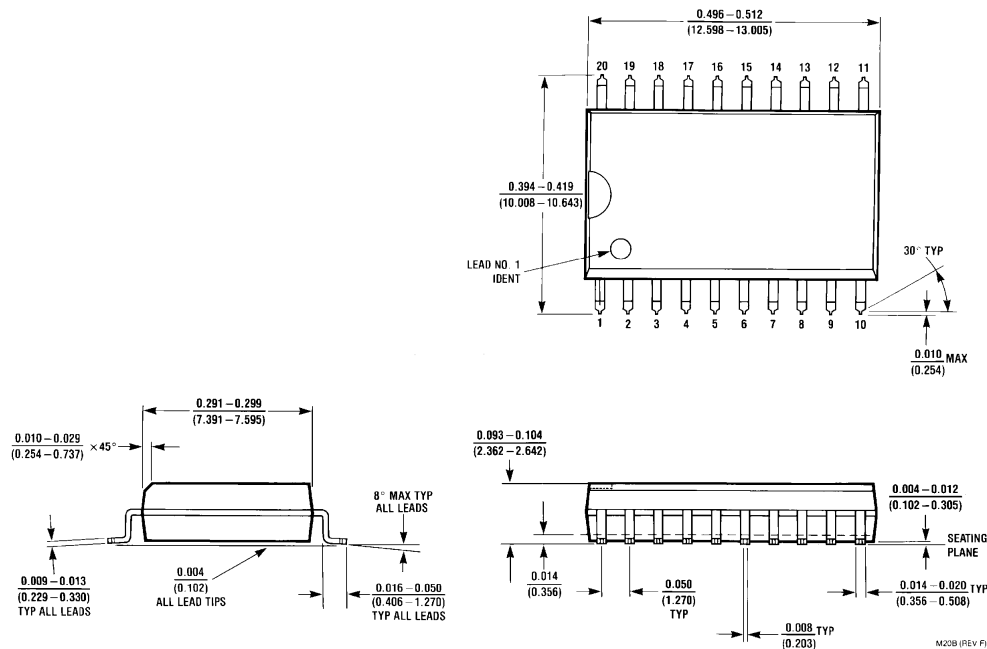
Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS273E
NS Package Number E20A



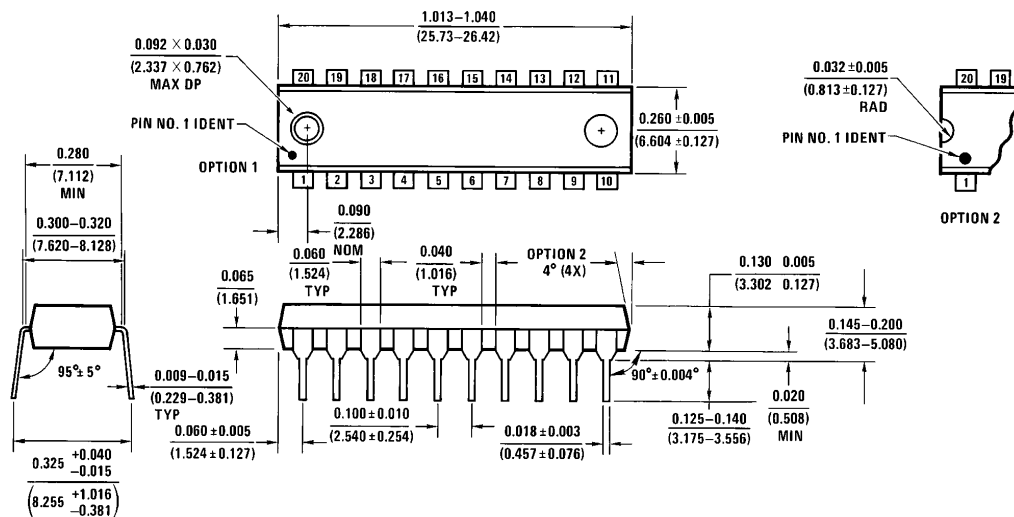
J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS273J
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

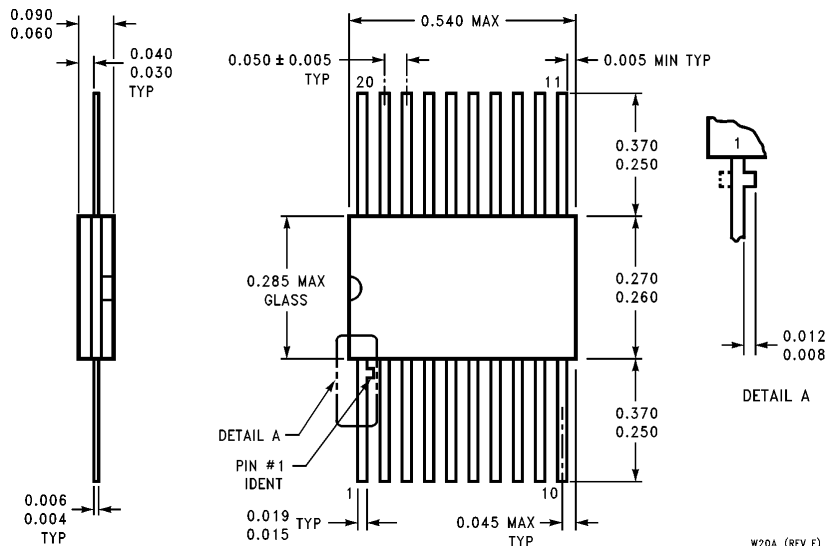


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS273M
NS Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS273N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS273W
NS Package Number W20A

W20A (REV E)

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408