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MOS FIELD EFFECT POWER TRANSISTOR

2SK1760

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1760 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 4.0 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 3 \text{ A}$)
- Low C_{iss} $C_{iss} = 790 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

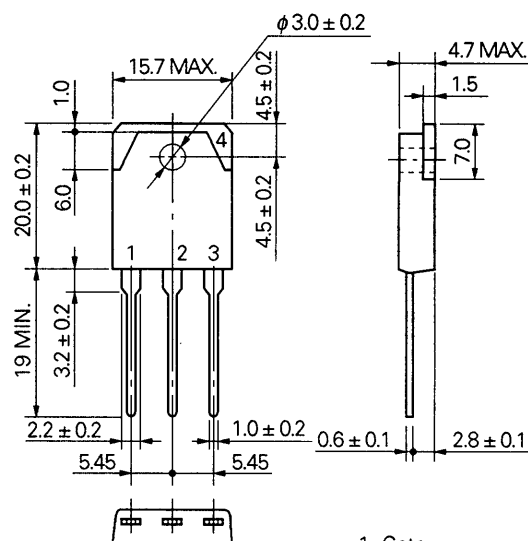
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DS}	900	V
Gate to Source Voltage	V_{GS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 5.0	A
Drain Current (pulse)	$I_{D(pulse)}^*$	± 10	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_T	100	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ\text{C}$

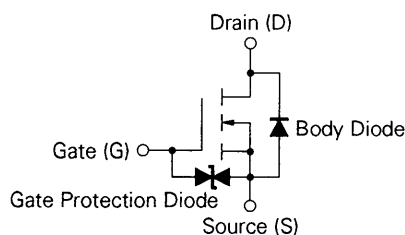
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

PACKAGE DIMENSIONS

(in millimeters)

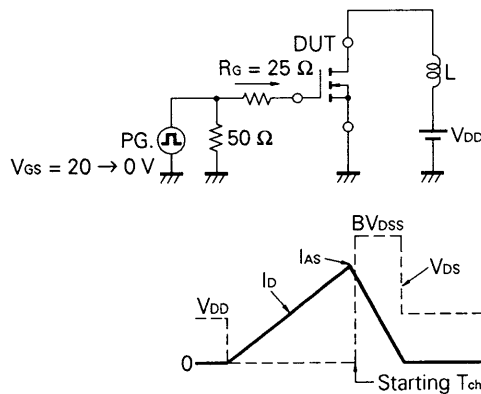
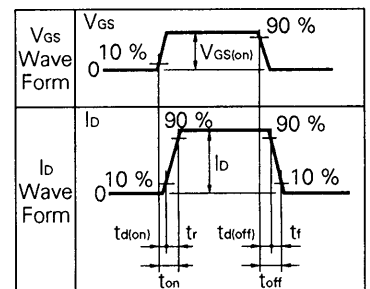
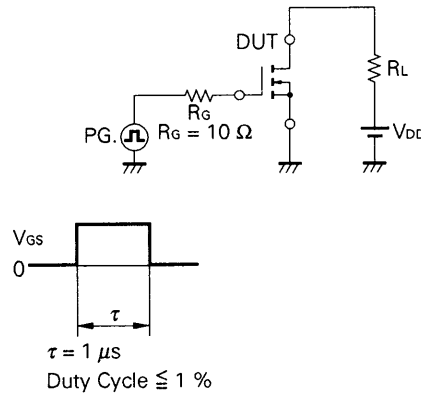
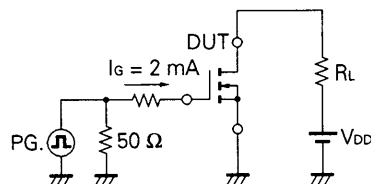


1. Gate
2. Drain
3. Source
4. Fin (Drain)

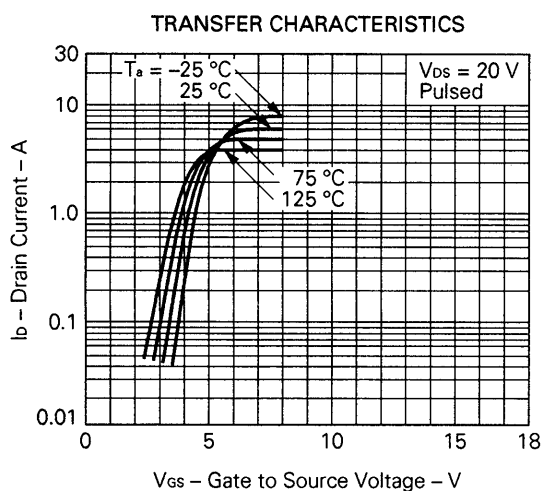
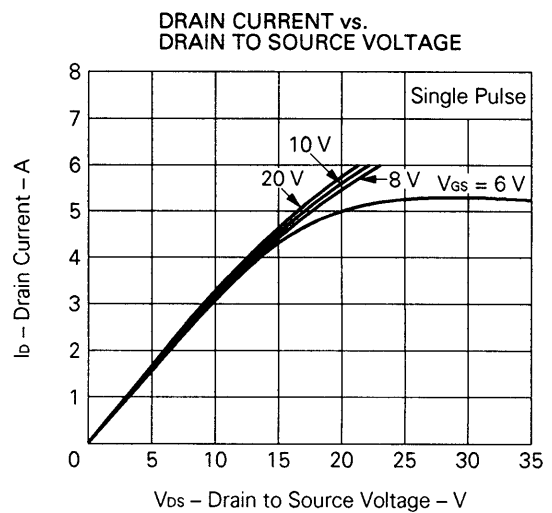
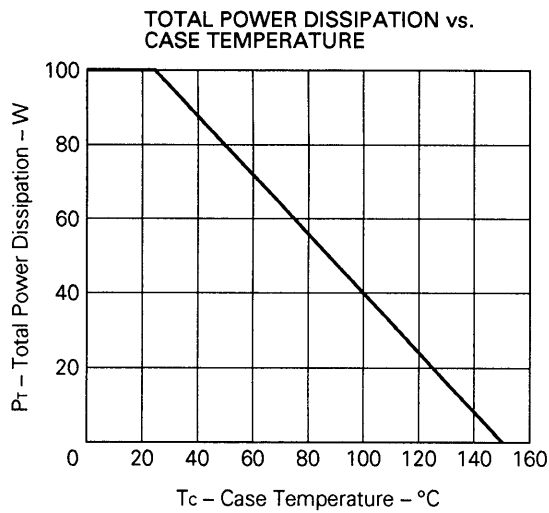
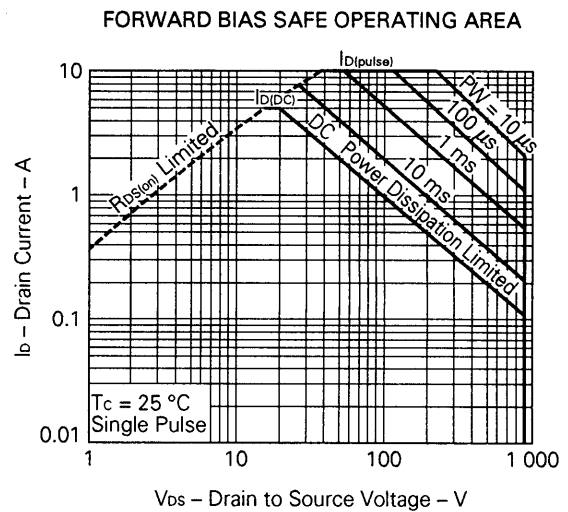
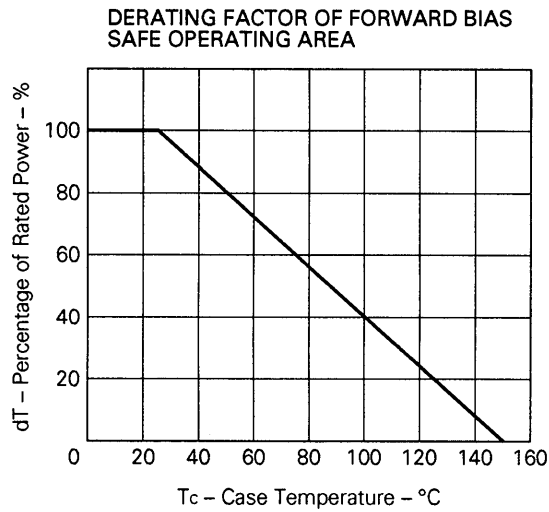


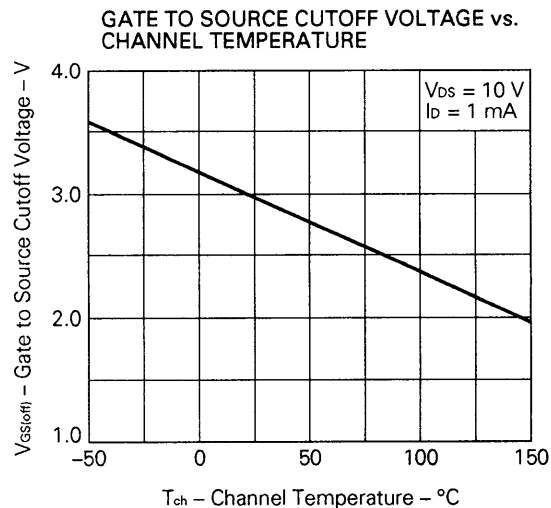
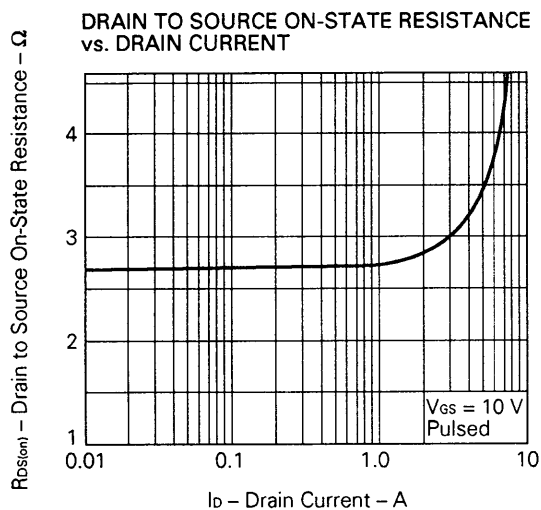
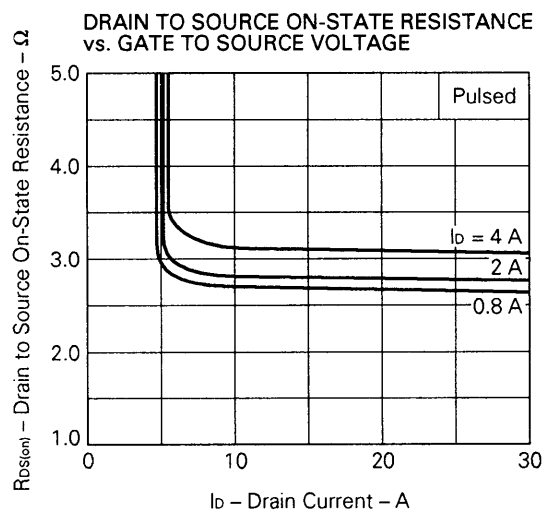
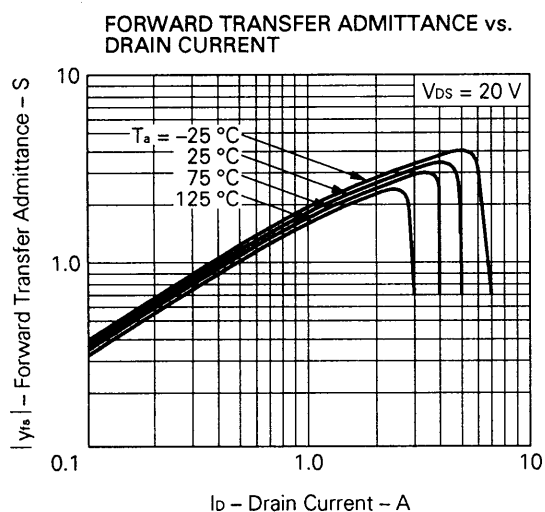
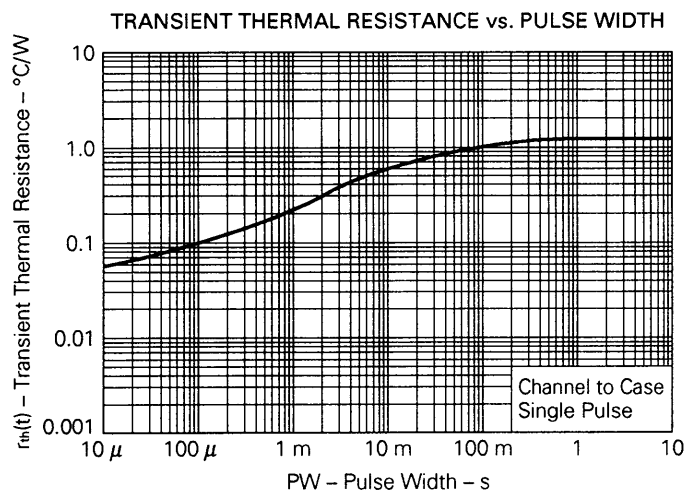
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

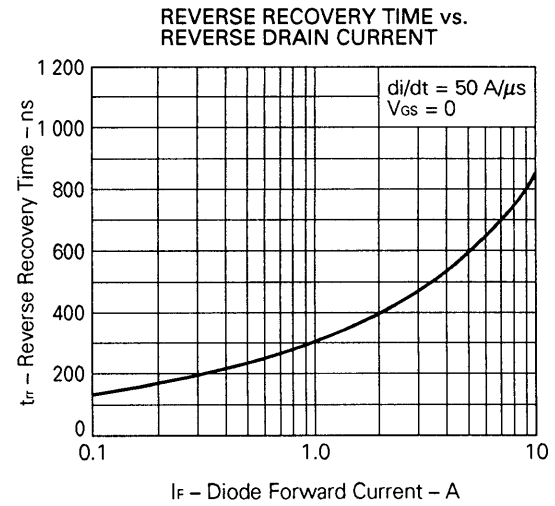
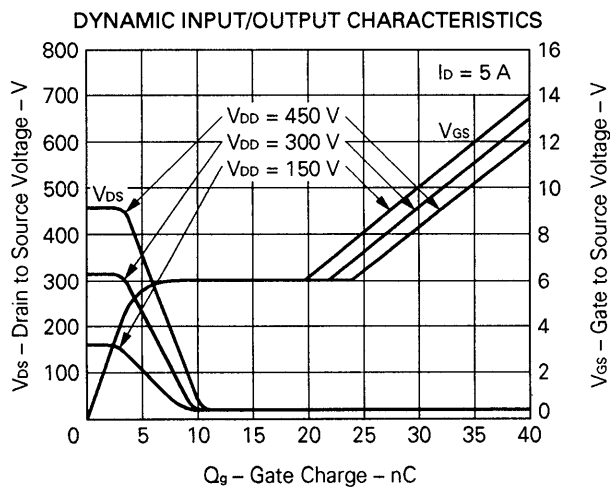
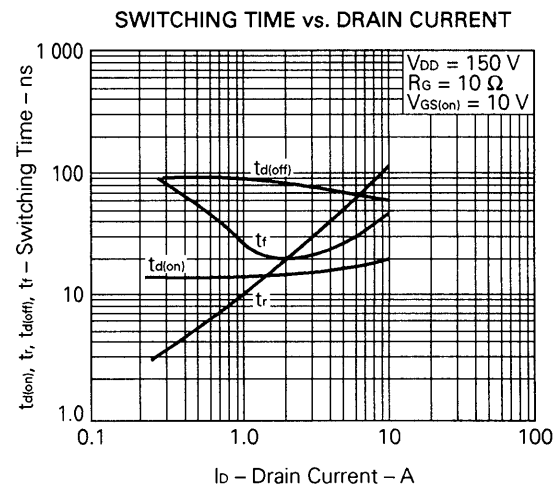
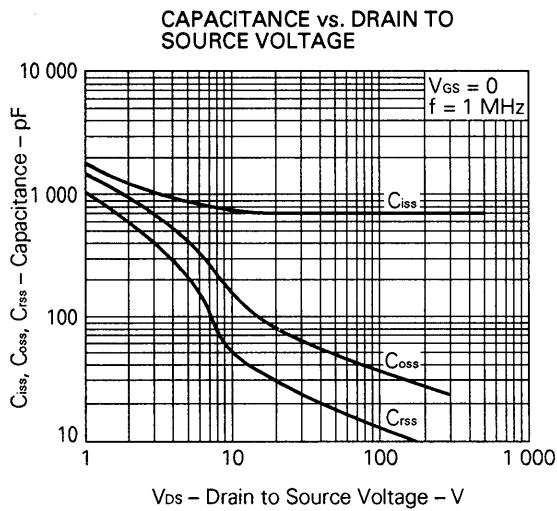
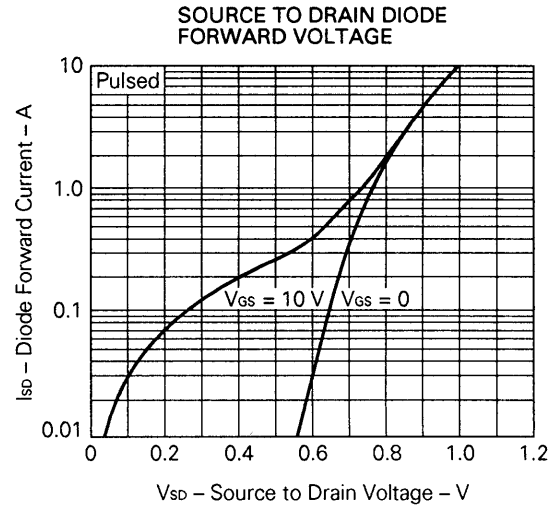
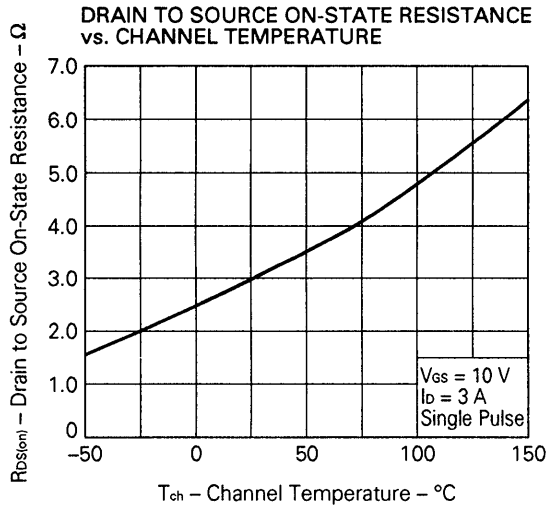
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		3.1	4.0	Ω	V _{GS} = 10 V, I _D = 3 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	1.0	3.1		S	V _{DS} = 20 V, I _D = 3 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 900 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		790		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		150		pF	
Reverse Transfer Capacitance	C _{rss}		60		pF	
Turn-On Delay Time	t _{d(on)}		15		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 3 A, R _G = 10 Ω R _L = 50 Ω
Rise Time	t _r		30		ns	
Turn-Off Delay Time	t _{d(off)}		80		ns	
Fall Time	t _f		25		ns	
Total Gate Charge	Q _G		34		nC	V _{GS} = 10 V I _D = 5 A V _{DD} = 450 V
Gate to Source Charge	Q _{GS}		6		nC	
Gate to Drain Charge	Q _{GD}		18		nC	
Diode Forward Voltage	V _{F(S-D)}		0.9		V	I _F = 5 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		660		ns	I _F = 5 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		4.5		μC	
Single Avalanche Current	I _{AS}			5.0	A	V _{DD} = 150 V, L = 100 μH R _G = 25 Ω, V _{GS} = 20 V → 0 Unclamped Starting T _{ch} = 25 °C

Test Circuit 1: Avalanche Capability**Test Circuit 2: Switching Time****Test Circuit 3: Gate Charge**

TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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