High Frequency, High Efficiency, Step-up DC/DC Converter

General Description

The RT9264 is a compact, high efficient, step-up DC/DC converter with current mode PWM control loop, providing stable and high efficient operations without external compensation.

The RT9264 suitable for 1 to 4 battery cells as well as USB power applications providing up to 400mA output current. The high switching rate minimized the size of external components.

A 300mA LDO is included in RT9264 to provide a secondary low noise output as well as an output current stop in the shutdown mode. RT9264 is provided in SOP-8 packages.

Ordering Information

RT9264□ □

- Package type
  S : SOP-8
- Operating temperature range
  C: Commercial standard

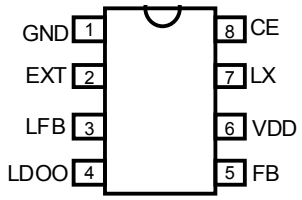
Features

- **400mA High Supply Capability**
- **90% Efficiency**
- **Switching Rate higher Than 1.4MHz**
- **Providing Flexibility for Using Internal and External Power Switches**
- **Built-in 300mA LDO, also for the Zero-Output-Current Shutdown Mode**
- **Boost DC-DC Integrating LDO for Up-Down Regulation**
- **8-Pin SOP Package**

Applications

- Portable Instrument
- ADSL Modem
- USB Devices

Pin Configurations

Part Number	Pin Configurations
RT9264CS (Plastic SOP-8)	TOP VIEW 

Typical Application Circuit

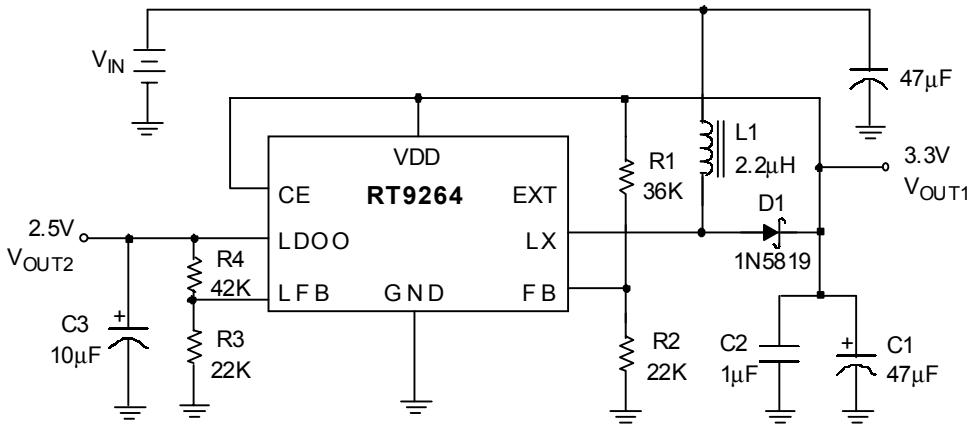


Fig. 1 RT9264 Typical Application for Portable Instruments

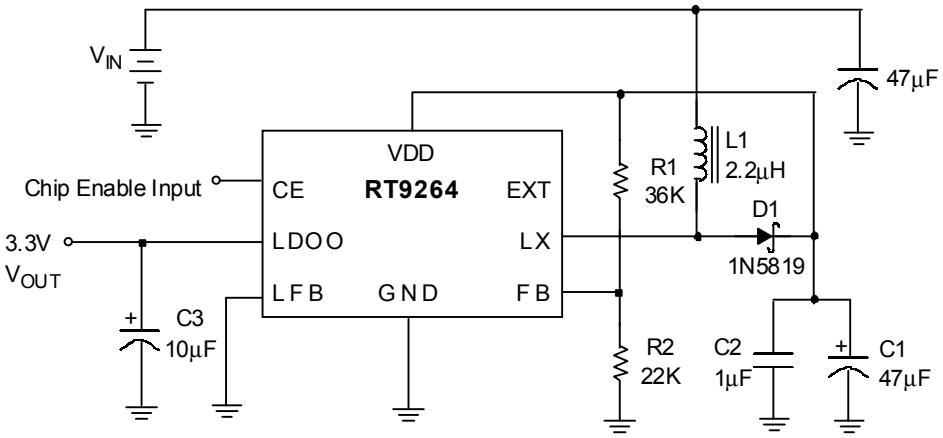


Fig. 2 Application Circuit with Zero-Output-Current Shutdown Mode Control

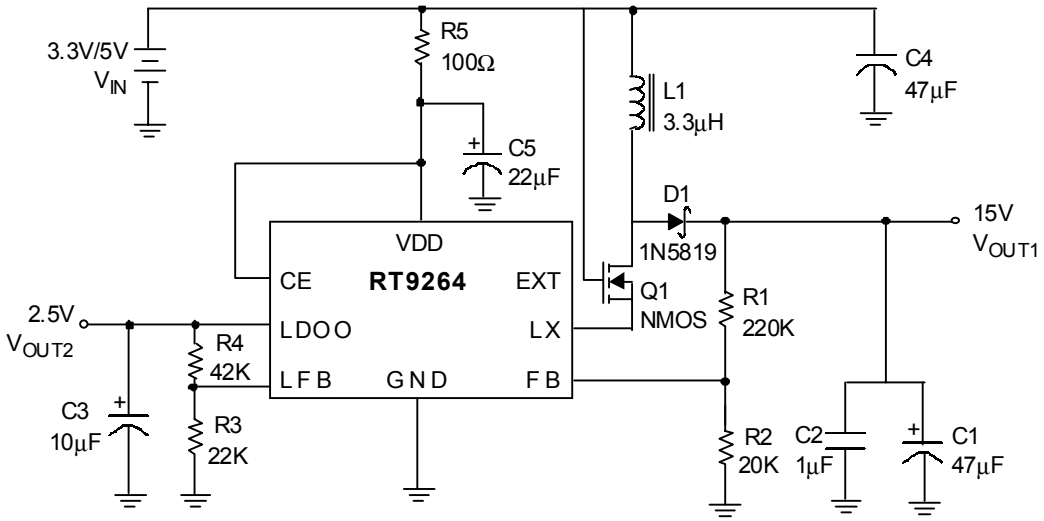
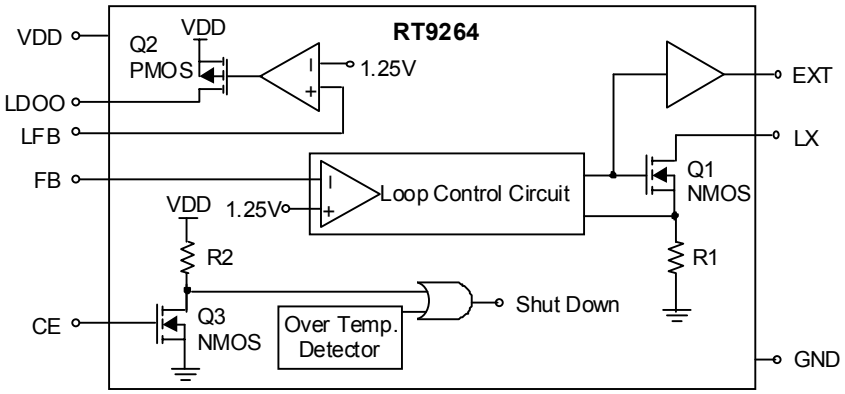


Fig. 3 High Voltage Application

Pin Description

Pin No.	Pin Name	Pin Function
1	GND	Ground
2	EXT	Output pin for driving external NMOS or NPN When driving an NPN, a resistor should be added for limiting base current.
3	LFB	Feedback pin of the built-in LDO (Internal Vref = 0.86V)
4	LDOO	Voltage output pin of the built-in LDO
5	FB	Feedback input pin Internal reference voltage for the error amplifier is 1.25V.
6	VDD	Input positive power pin of RT9264
7	LX	Pin for switching
8	CE	Chip enable RT9264 gets into shutdown mode when CE pin set to low.

Function Block Diagram



Absolute Maximum Ratings

- Supply Voltage ---------- -0.3V to 6V
- LX Pin Switch Voltage ---------- -0.3V to (VDD + 0.8V)
- LDO Output Voltage ---------- -0.3V to (VDD + 0.3V)
- Other I/O Pin Voltages ---------- -0.3V to (VDD + 0.3V)
- LX Pin Switch Current ---------- 2.5A
- EXT Pin Driver Current ---------- 30mA
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.625W
- Package Thermal Resistance
  SOP-8, θ_{JA} ---------- 160°C/W
- Operating Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- -65°C ~ +150°C

Electrical Characteristics

(V_{IN} = 3.3V, VDD set to 5V, Load Current = 0, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating VDD Range	V_{DD}		1	--	6	V
No Load Current I (V_{IN})	$I_{NO\ LOAD}$	V_{IN} = 3.3V, V_{OUT} = 5V	--	3	--	mA
Switch-off Current I (VDD)	$I_{SWITCH\ OFF}$	V_{IN} = 6V	--	1	--	mA
Shutdown Current I (V_{IN})	I_{OFF}	CE Pin = 0V, V_{IN} = 4.5V	--	0.1	1	μA
Feedback Reference Voltage	V_{REF}	Close Loop, VDD = 3.3V	1.225	1.25	1.275	V
Feedback Reference Voltage for LDO	V_{REF}	Close Loop, VDD = 3.3V	0.843	0.86	0.877	V
Switching Rate	F_S	VDD = 5V	1.4	--	2.8	MHz
Maximum Duty	D_{MAX}	VDD = 5V	--	80	--	%
LX ON Resistance		VDD = 5V	--	0.25	--	Ω
Current Limit Setting	I_{LIMIT}	VDD = 5V	--	2	--	A
EXT ON Resistance to VDD		VDD = 5V	--	30	--	Ω
EXT ON Resistance to GND		VDD = 5V	--	20	--	Ω
Line Regulation	ΔV_{LINE}	V_{IN} = 3 ~ 4V, I_L = 1mA	--	20	--	mV/V
Load Regulation	ΔV_{LOAD}	V_{IN} = 3.3V, I_L = 1 ~ 50mA	--	0.5	--	mV/mA
LDO PMOS ON Resistance		VDD = 5V	--	1	1.5	Ω
LDO Drop Out Voltage	V_{DROP}	VDD = 5V, IL = 100mA	--	70	--	mV
CE Pin Trip Level		VDD = 5V	0.2	0.8	1.4	V
Temperature Stability for FB, LFB, LBI	T_S	Guaranteed by Design	--	50	--	ppm/°C
Thermal Shutdown	T_{SD}	Guaranteed by Design	--	165	--	°C
Thermal Shutdown Hysterises	ΔT_{SD}	Guaranteed by Design	--	10	--	°C

Application Note

Output Voltage Setting

Referring to application circuits Fig.1 to Fig.3, the output voltage of the switching regulator (V_{OUT1}) can be set with Eq.1.

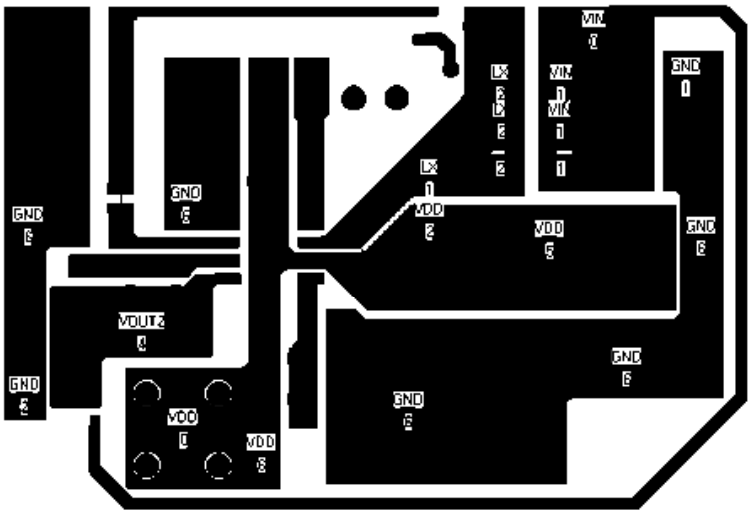
The LDO output voltage can be set with Eq.2.

$$V_{OUT1} = (1+\frac{R1}{R2})\times 1.25V \quad \text{Eq.1}$$

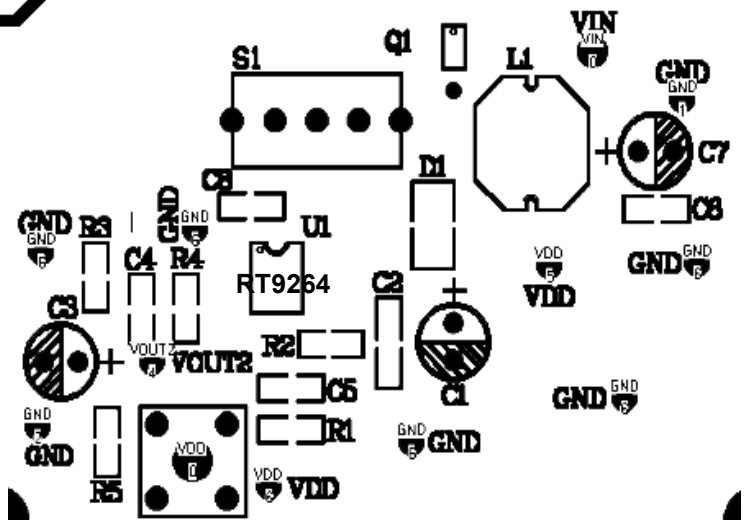
$$V_{OUT2} = (1+\frac{R4}{R3})\times 0.86V \quad \text{Eq.2}$$

Layout Guide

- A full GND plane without gap break.
- V_{OUT1} to GND noise bypass – Short and wide connection for C2 to Pin1 and Pin6.
- V_{IN} to GND noise bypass – Add a 100μF capacitor close to L1 inductor, when VIN is not an idea voltage source.
- Minimized FB/LFB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.
- The following diagram is an example of 2-layer board layout for application circuits Fig.1 and Fig.2.

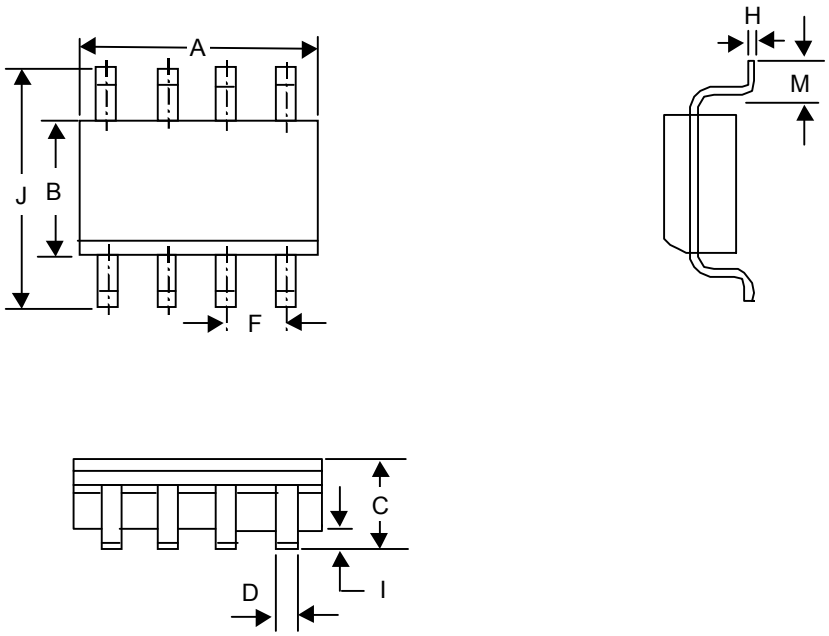


First Layer



Second Layer (Full GND Plane)

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

8–Lead SOP Plastic Package

RICHTEK TECHNOLOGY CORP.
Headquarter
6F, No. 35, Hsintai Road, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5510047 Fax: (8863)5537749

RICHTEK TECHNOLOGY CORP.
Taipei Office (Marketing)
8F-1, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek-ic.com.tw