FUJITSU

UV ERASABLE 8192-BIT READ ONLY MEMORY

MB 8518H

MOS 8192-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

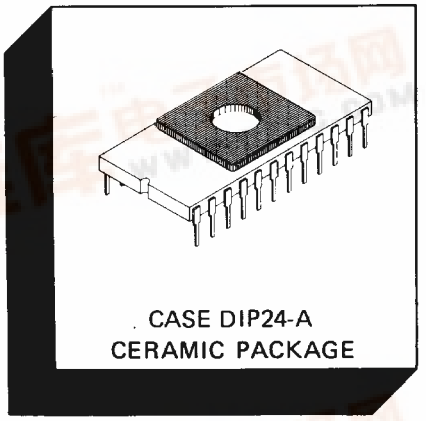
September 1978

The Fujitsu MB 8518 is a high speed 8192-bit static N-channel MOS erasable and electrically programmable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 24-pin dual-in-line package with a transparent lid is used to package the MB 8518. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MB 8518 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. A pin-for-pin equivalent mask programmed ROM, the Fujitsu MB 8308, is available for large volume requirements.

- 1024 words by 8 bits organization, fully decoded
- Fast programming (typ. 100 sec. for all 8192 bits)
- Low power requirement (only one high-level pulse required)
- No clocks required (fully static operation)
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Chip Select ($\overline{CS}$) lead for simplified memory expansion



CASE DIP24-A
CERAMIC PACKAGE

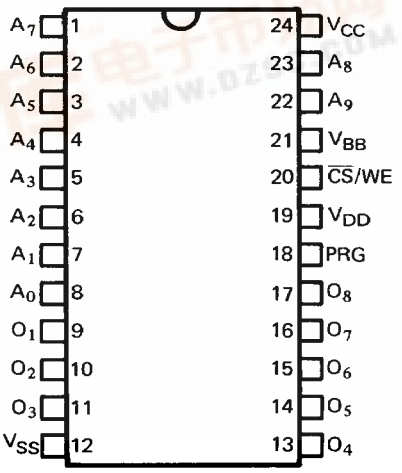
- Standard (+12V and ±5V) power supplies
- Standard 24-pin DIP package
- Interchangeable with Intel 2708

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to + 85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs (Except PRG and $\overline{CS}$/WE) with Respect to V_{BB}	V_{IN1},V_{OUT}	−0.3 to +15	V
Program Input with Respect to V_{BB}	V_P	−0.3 to +35	V
$\overline{CS}$/WE with Respect to V_{BB}	V_{IN2}	−0.3 to +20	V
V_{CC} and V_{SS} with Respect to V_{BB}	V_{CC},V_{SS}	−0.3 to +15	V
V_{DD} with Respect to V_{BB}	V_{DD}	−0.3 to +20	V
Power Dissipation	P_D	1.5	W

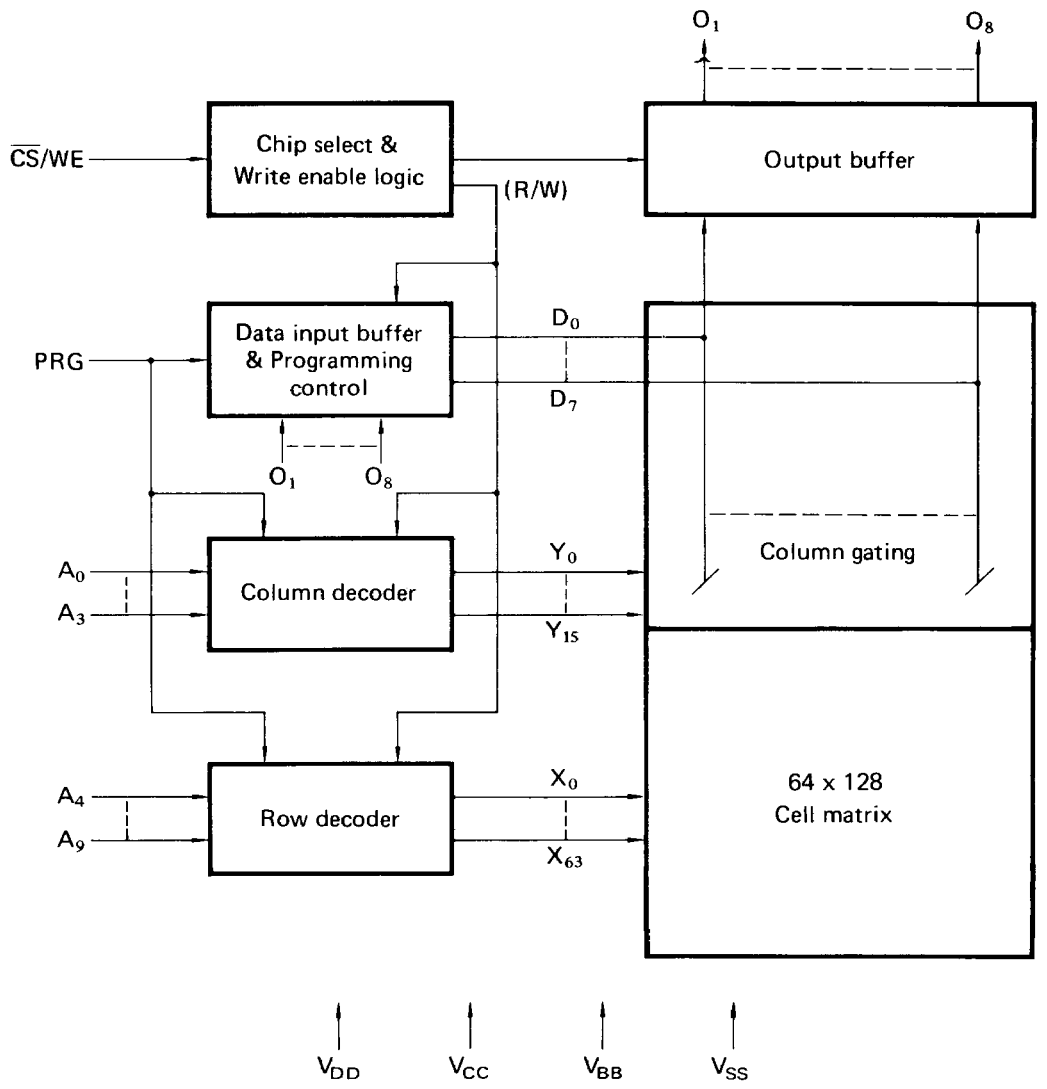
Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than

Fig. 1 – MB 8518 BLOCK DIAGRAM



FUNCTIONS AND PIN CONNECTIONS

Function (Pin No.) / Mode	Address Input (1~8, 22, 23)	Data I/O (9~11,13~17)	V_{SS} (GND) (12)	PRG (Program) (18)	V_{DD} Supply (19)	$\overline{CS}$/WE (20)	V_{BB} Supply (21)	V_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	GND	GND	+12V	V_{IL}	–5V	+5V
Deselect	DON'T CARE	HIGH Z	GND	GND	+12V	V_{IH}	–5V	+5V
Program	A	D	GND	PULSED	+12V	V_{IL}	–5V	+5V

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{DD}	11.4	12	12.6	V	0°C to +70°C
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Supply Voltage	V_{SS}	–	0.0	–	V	
Supply Voltage	V_{BB}	– 4.75	– 5.0	– 5.25	V	
Input High Voltage	V_{IH}	3.0	–	V_{CC}+1	V	
Input Low Voltage	V_{IL}	V_{SS}	–	0.65	V	

STATIC CHARACTERISTICS (Recommended operating conditions unless otherwise noted, and pin 18 PRG must be tied to V_{SS} during read operation.)

Parameter	Symbol	Min	Typ	Max	Unit
Address and Chip Select Input Load Current (V_{IN}=5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT}=5.25V, $\overline{CS}$/WE=5V)	I_{LO}	—	—	10	μA
V_{DD} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=5V)	I_{DD}*	—	50	65	mA
V_{CC} Supply Current (All Inputs=V_{IL}, $\overline{CS}$/WE=5V)	I_{CC}*	—	7	10	mA
V_{BB} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=5V)	I_{BB}*	—	30	45	mA
Output Low Voltage (I_{OL}=1.6mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH}=–100μA)	V_{OH1}	3.7	—	—	V
Output High Voltage (I_{OH}=–1mA)	V_{OH2}	2.4	—	—	V
Power Dissipation (T_A=70°C)	P_D	—	—	800	mW

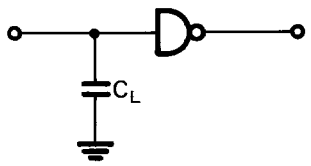
***Note:** Typical values are measured at nominal voltage and T_A=25°C; max. values at T_A=0°C.

CAPACITANCE (T_A=25°C; f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN}=0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT}=0V)	C_{OUT}	—	8	12	pF

Fig. 2 – DYNAMIC TEST CONDITIONS

Input Pulse Levels:	0.65V to 3.0V
Input Rise and Fall Time:	≦20ns
Timing Measurement Reference Levels:	0.8V and 2.8V for inputs
	0.8V and 2.4V for outputs
Output Load:	1 TTL gate and C_L=100pF



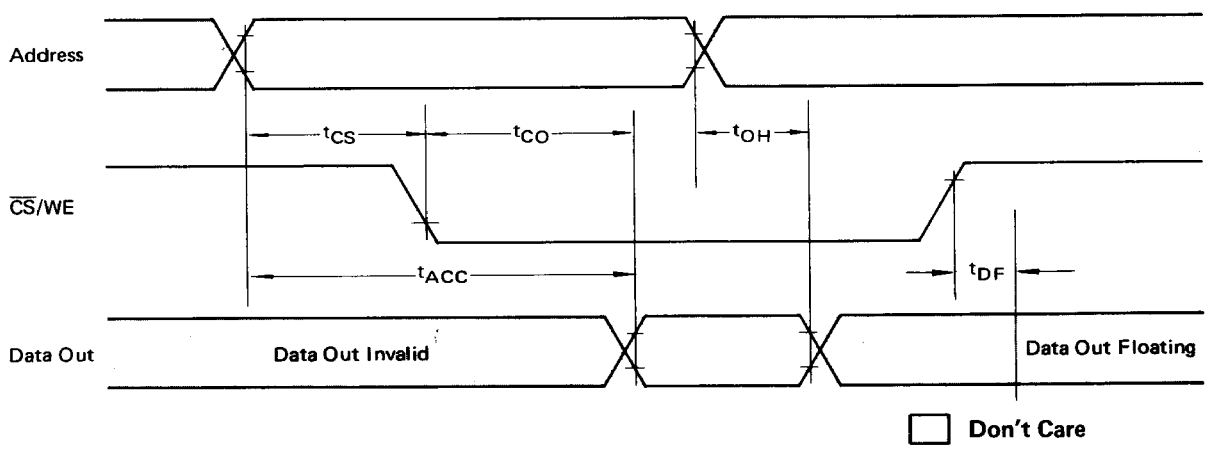
DYNAMIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit
Address to Output Delay	t_{ACC}	–	–	450	ns
Chip Select to Output Delay	t_{CO}	–	–	120	ns
Chip Deselect to Output Float	t_{DF}	0	–	120	ns
Address to Output Hold	t_{OH}	0	–	–	ns
Chip Select Delay	t_{CS}*	–	–	330	ns

***Note:** $t_{ACC}=t_{CS}+t_{CO}$ at $t_{CS} > 330$ns, and $t_{ACC}=450$ns (max.) at $t_{CS} \leqq 330$ns.

OPERATION TIMING DIAGRAM



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs V_{DD} SUPPLY VOLTAGE

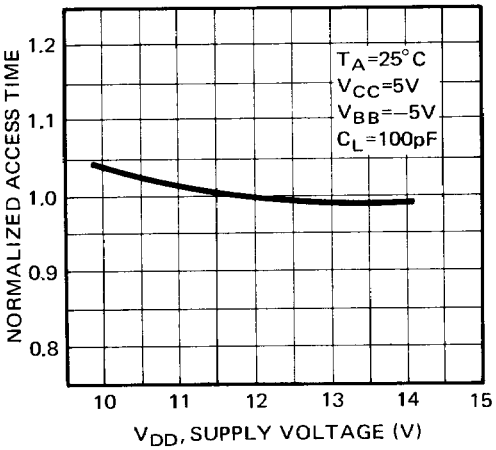


Fig. 4 – NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

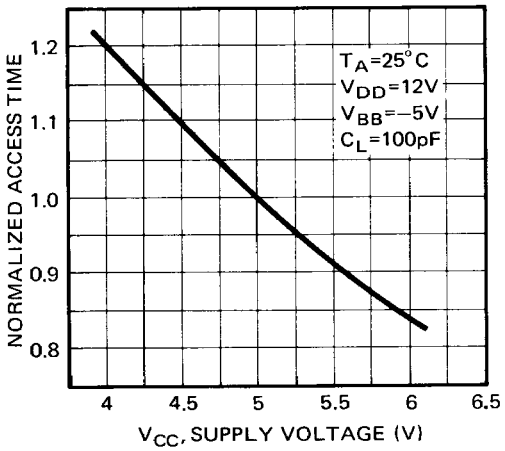


Fig. 5 – NORMALIZED ACCESS TIME vs V_{BB} SUPPLY VOLTAGE

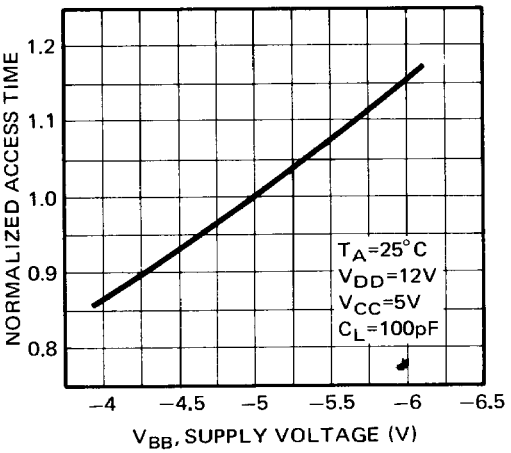


Fig. 6 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

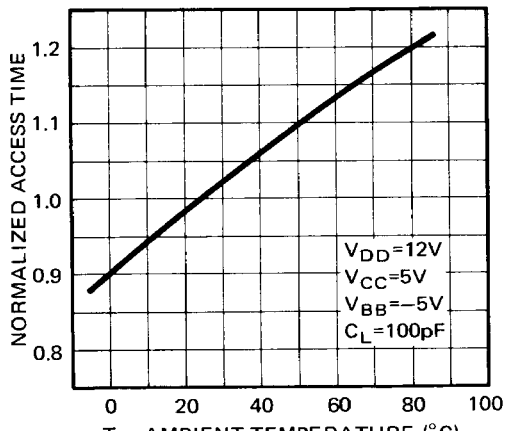


Fig. 7 – NORMALIZED ACCESS TIME vs C_L LOAD CAPACITANCE

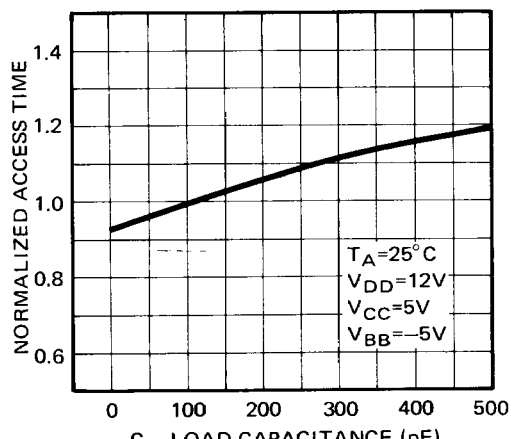


Fig. 8 – I_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

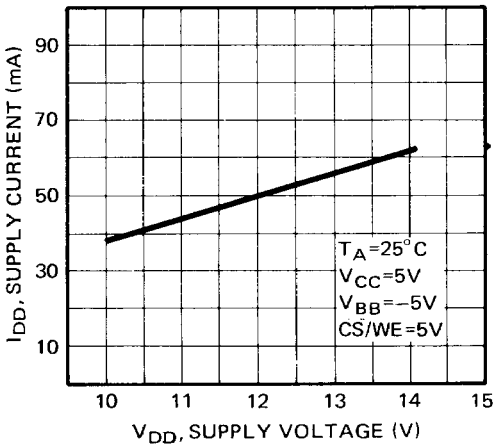


Fig. 9 – I_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

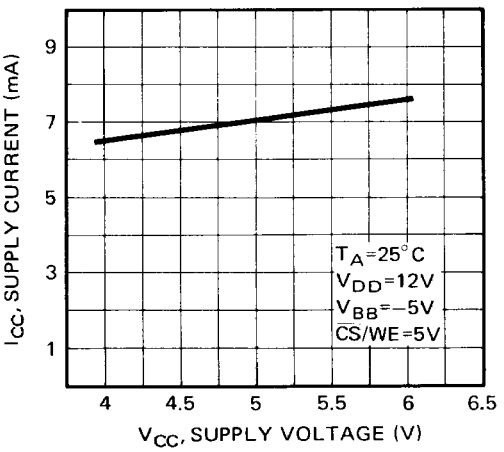


Fig. 10 – I_{BB} SUPPLY CURRENT vs V_{BB} SUPPLY VOLTAGE

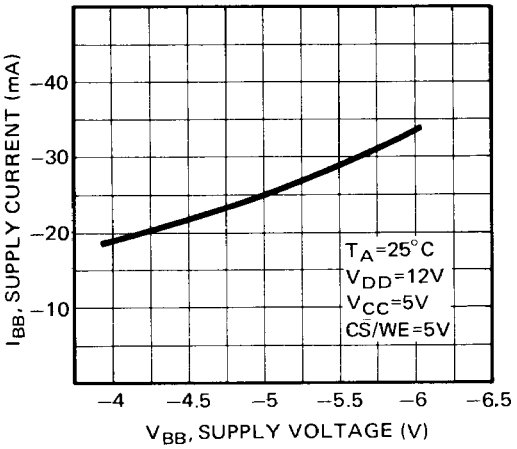


Fig. 11 – I_{OH} OUTPUT SOURCE CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

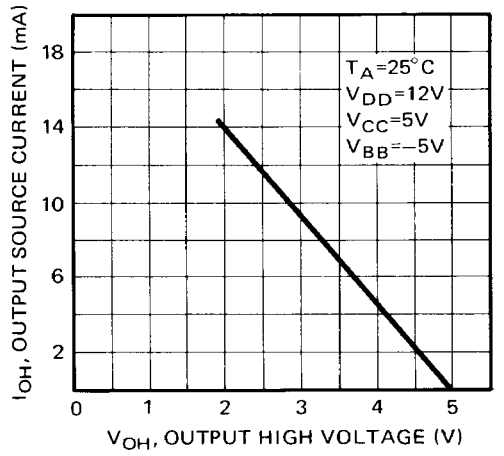


Fig. 12 – I_{OL} OUTPUT SINK CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

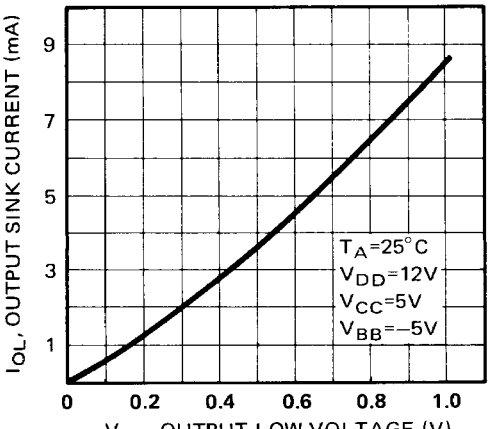
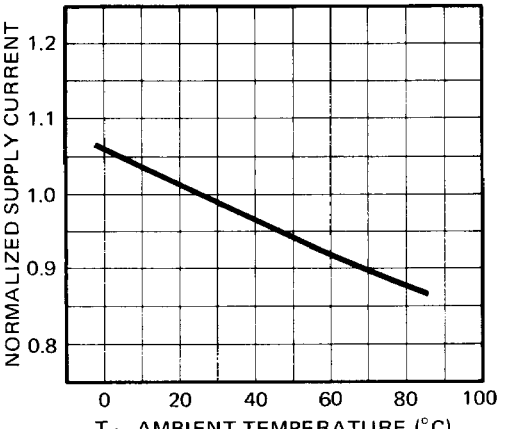


Fig. 13 – NORMALIZED SUPPLY CURRENT vs AMBIENT TEMPERATURE



PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MB 8518 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{THO}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

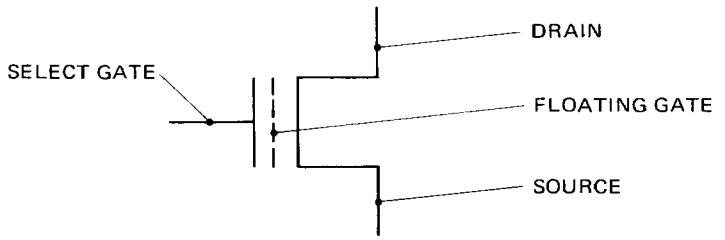
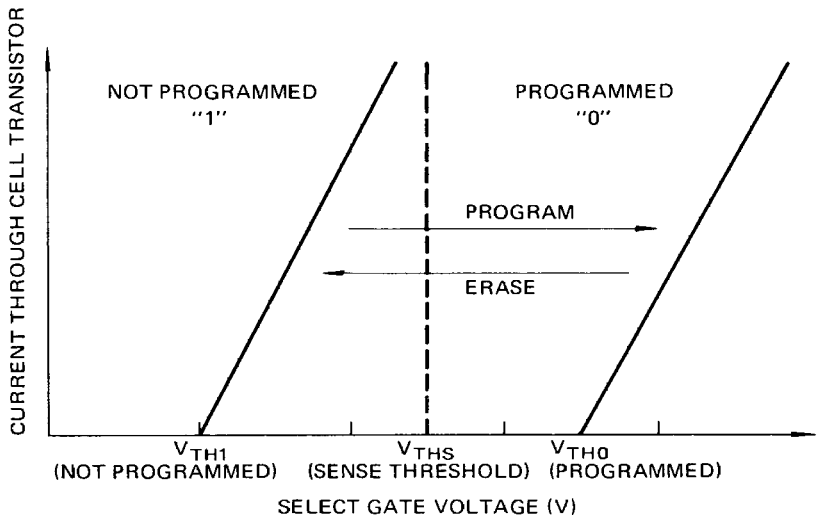


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Initially, and after each erasure, all bits are in the "1" (output high) state. Information is stored by programming a "0" into each desired bit location. Address and supply voltage (V_{DD}, V_{CC}, V_{BB} and V_{SS}) input levels used in the read mode of operation are also applicable in the programming mode. For programming operation, the circuit is set up by applying +12V to the $\overline{CS}$/WE lead (pin 20). The word address is then selected in the same manner as in the read mode, with data to be programmed applied 8 bits in parallel to the data lines (O_1~O_8). After address and data set up, one program pulse (V_P) per address is applied to the Program input (pin 18). One pass through all addresses to be programmed is defined as a program loop. The number of loops required (N) is a function of the program pulse width (t_{PW}) according to the formula $N \times t_{PW} \geqq 100$ msec. For programming verification, program loops and read loops may be alternated as shown in "Read/Program/Read Transitions Diagram."

During programming, the selected row and column lines are pulsed to approximately 22 volts, and the floating gate is charged (as described previously). It is the presence of these 22V pulses on the interconnected gates that leads to the requirement that *all addresses must be programmed sequentially; programming of single words or small blocks of words is not allowed,* as transients may be generated that could partially alter the charge state of cells not being programmed.

ERASING

The MB 8518 can be erased by exposure to high-intensity, shortwave ultraviolet light at a wavelength of 2537Å. The recommended integrated dosage (UV intensity x exposure time) is 10Wsec./cm^2. Normally, commercial ultraviolet lamps should be used without shortwave filters, with the device to be erased placed one inch (2 to 3cm) away from the lamp tube. It is suggested that a guard band of 3~4 times the

(cont.)

PROGRAMMING/ERASING INFORMATION (continued)

minimum required period for erasure be used, the minimum period being the time which appears to erase all bits. The guard band will ensure erasure at temperature and voltage extremes. Typical guard band erase times for various UV source power ratings are: typically 10 minutes for 12,000μW/cm^2; typically 30 minutes for 6,000μW/cm^2.

SUPPLEMENTARY INFORMATION

Programming can be performed in accordance with the procedure described in "Programming." A recommended circuit for programming pulse generation is shown in Fig. 16. The program pulse high voltage (V_{PH}) source must sink more than 20mA, and the program pulse low voltage (V_{PL}) source should drive more than 8mA.

The width of the program pulse can vary anywhere from 0.1 to 1.0 msec. The number of loops (N) can vary from a minimum of 100 (t_{PW}=1.0 msec.) to a maximum of more than 1,000 (t_{PW}=0.1 msec.), depending on the value selected for t_{PW}. Remember, however, *there must be "N" successive loops through all 1024 addresses. It is incorrect to apply "N" program pulses to one address, change to the next address, and again apply "N" program pulses.*

With reference to the timing diagram, optimum or more efficient programming is achieved when:

$t_{CSS} = t_{AS} = t_{DS} = 10$ μsec.
$t_{PW} = 1.0$ msec.
$t_{AH} = t_{DH} = 1.0$ μsec.
$t_{PR} = t_{PF} = 0.5$ μsec.

Thus the time for one address is:

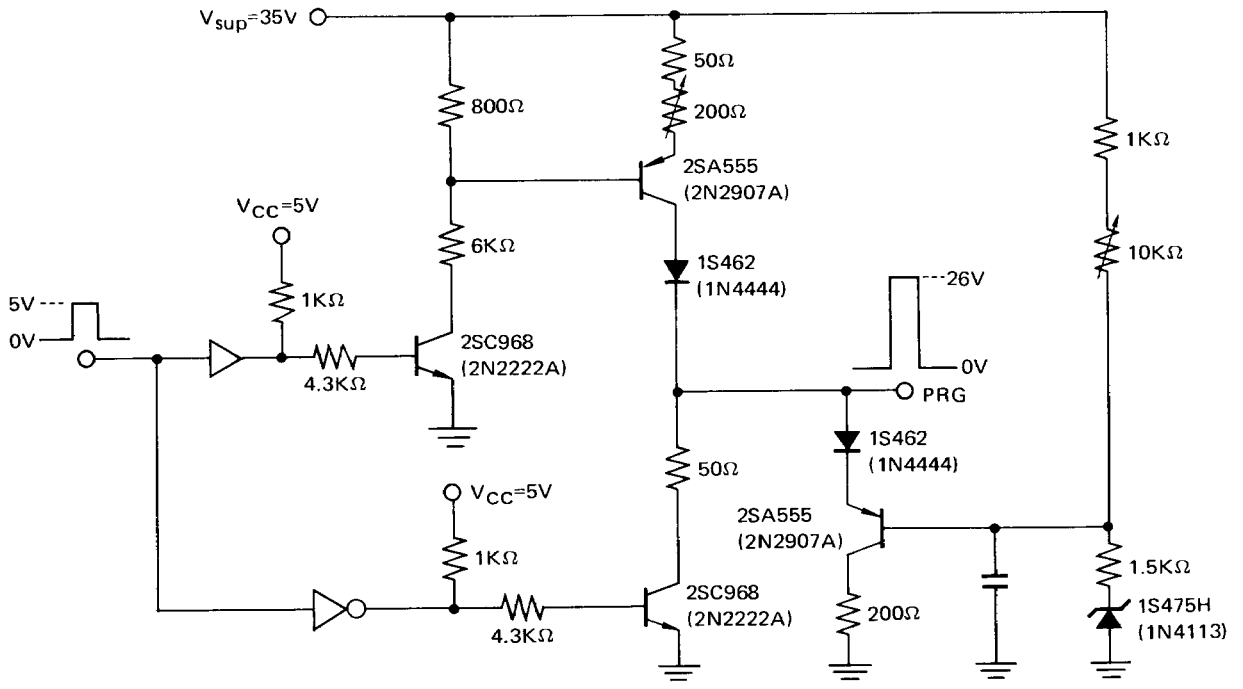
$t_{AS} + t_{PR} + t_{PW} + t_{PF} + t_{AH}$ = 1.012 msec.

For 100 loops and 1024 addresses, the total time to program an entire device will be:

1.012 msec./address x 100 loops x 1024 addresses = 103.6 sec.

Note that the program pulse duty cycle is approximately 99%. Regardless of the length of the program pulse, the requirement for making successive passes through all addresses cannot be eliminated.

Fig. 16 — SAMPLE PROGRAM PULSE DRIVER CIRCUIT



STATIC SPECIFICATIONS (T_A=25°C, V_{DD}=12V±5%, V_{CC}=5V±5%, V_{SS}=0V, V_{BB}=−5V±5%)

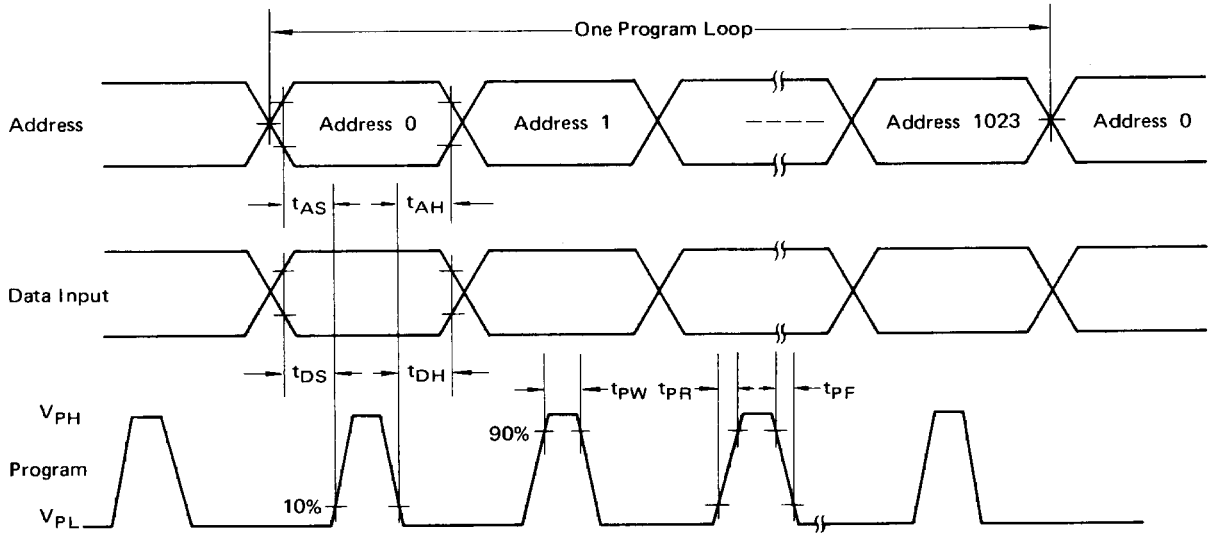
Parameter	Symbol	Min	Typ	Max	Unit
Input High Voltage for Address and Data	V_{IH}	3.0	—	V_{CC}+1	V
Input Low Voltage for Address and Data	V_{IL}	V_{SS}	—	0.65	V
Address and Data Input Load Current (V_{IN}=5.25V, $\overline{CS}$/WE=11.4V)	I_{LIA}, I_{LID}	—	—	10	μA
$\overline{CS}$/WE Input Load Current ($\overline{CS}$/WE=12.6V)	I_{LIW}	—	—	10	μA
$\overline{CS}$/WE Input High Voltage	V_{IHW}	11.4	—	12.6	V
V_{DD} Supply Current (All Inputs=V_{IH}, PRG=V_{PL}, $\overline{CS}$/WE=11.4V)	I_{DDW}	—	—	78	mA
V_{CC} Supply Current (All Inputs=V_{IL}, $\overline{CS}$/WE=11.4V)	I_{CCW}	—	—	12	mA
V_{BB} Supply Current (All Inputs=V_{IH}, $\overline{CS}$/WE=11.4V)	I_{BBW}	—	—	50	mA
Program Pulse Source Current	I_{PL}	—	—	8	mA
Program Pulse Sink Current	I_{PH}	—	—	20	mA
Program Pulse Low Voltage	V_{PL}	V_{SS}	—	1	V
Program Pulse High Voltage	V_{PH}	—	—	27	V
Program Pulse Height	—	25	—	27	V

DYNAMIC SPECIFICATIONS (T_A=25°C)

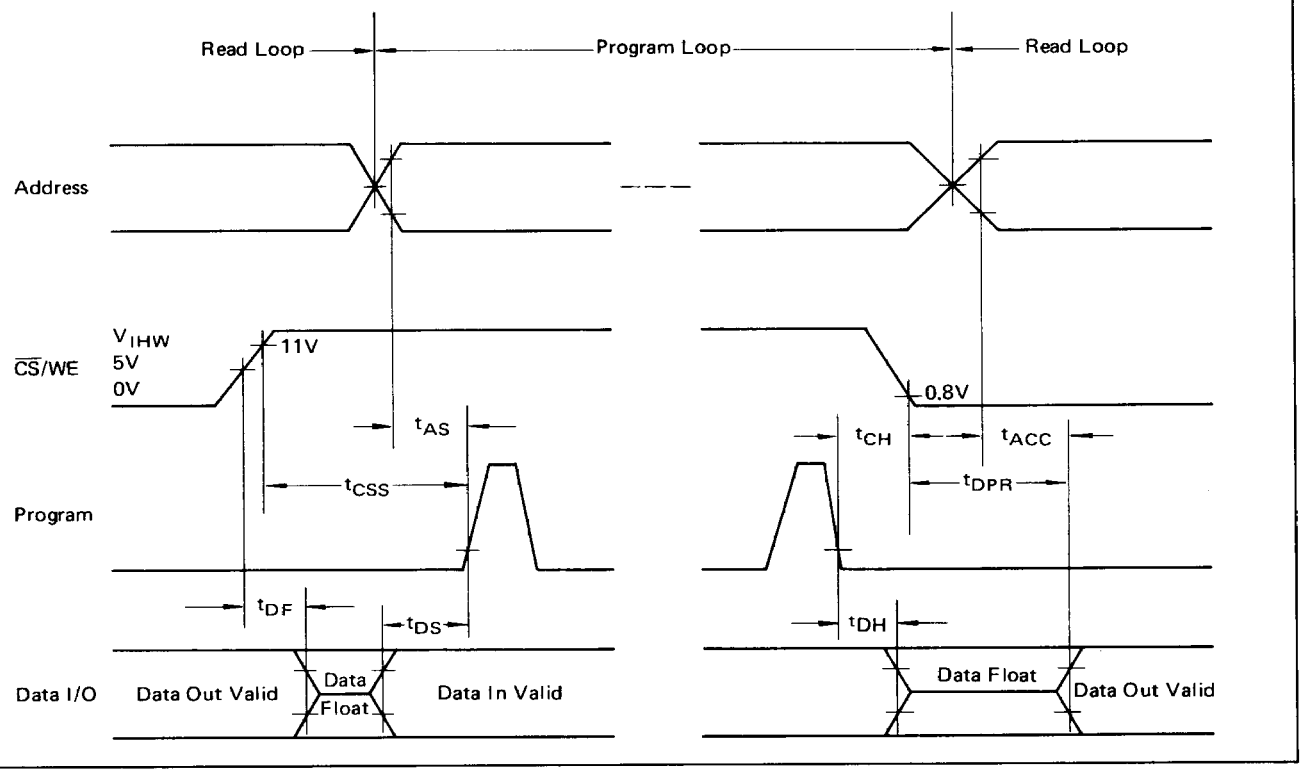
Parameter	Symbol	Min	Typ	Max	Unit
Address Set Up Time	t_{AS}	10	—	—	μs
$\overline{CS}$/WE Set Up Time	t_{CSS}	10	—	—	μs
Data Set Up Time	t_{DS}	10	—	—	μs
Address Hold Time	t_{AH}	1	—	—	μs
$\overline{CS}$/WE Hold Time	t_{CH}	0.5	—	—	μs
Data Hold Time	t_{DH}	1	—	—	μs
Chip Deselect to Output Float Delay	t_{DF}	0	—	120	ns
Program to Read Delay	t_{DPR}	—	—	10	μs
Program Pulse Width	t_{PW}	0.1	—	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	—	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	—	2.0	μs

PROGRAMMING/ERASING INFORMATION (continued)

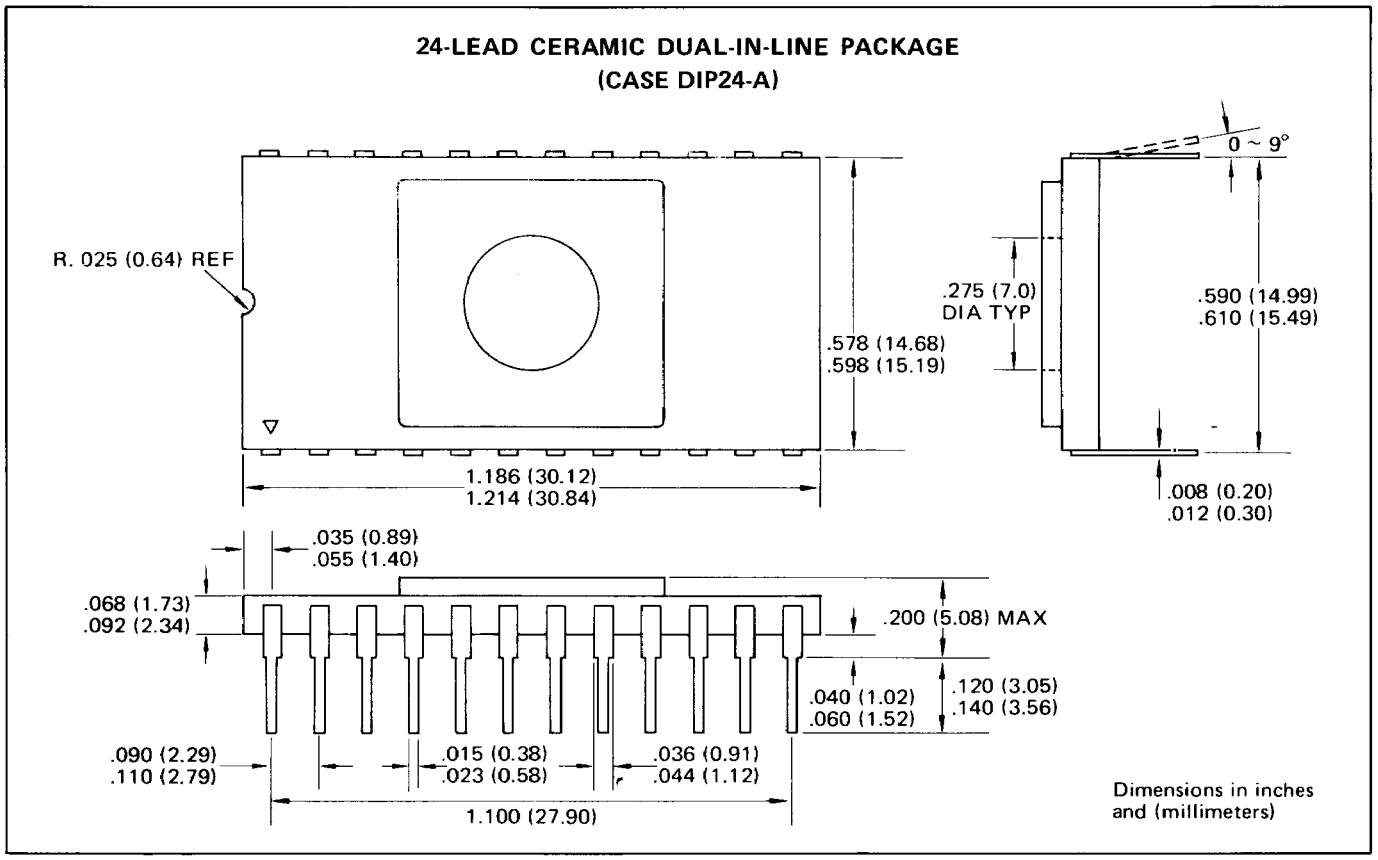
PROGRAM MODE TIMING DIAGRAM



READ/PROGRAM/READ TRANSITIONS DIAGRAM



PACKAGE DIMENSIONS



Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.