

SONY

CXD1177Q

8-bit 40MSPS YC 2-channel D/A Converter

Description

The CXD1177Q is an 8-bit high-speed D/A converter for video band use. It has an input/output equivalent to 2 channels of Y and C. It is suitable for use of digital TV, graphic display, and others.

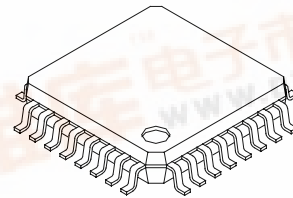
Features

- Resolution 8-bit
- Maximum conversion speed 40MSPS
- YC 2-channel input/output
- Differential linearity error ± 0.3 LSB
- Low power consumption 160 mW (200 Ω load at 2 Vp-p output)
- Single 5 V power supply
- Low glitch noise
- Stand-by function

Structure

Silicon gate CMOS IC

32 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage AVDD, DVDD 7 V
- Input voltage (All pins)

VIN	VDD +0.5 to VSS -0.5	V
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- Output current (Every each channel)

IOUT	0 to 15	mA
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- Storage temperature

Tstg	-55 to +150	°C
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Recommended Operating Conditions

- Supply voltage AVDD, AVSS 4.75 to 5.25 V
- | | | |
|------------|--------------|---|
| DVDD, DVSS | 4.75 to 5.25 | V |
|------------|--------------|---|
- Reference input voltage

VREF	2.0	V
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- Clock pulse width

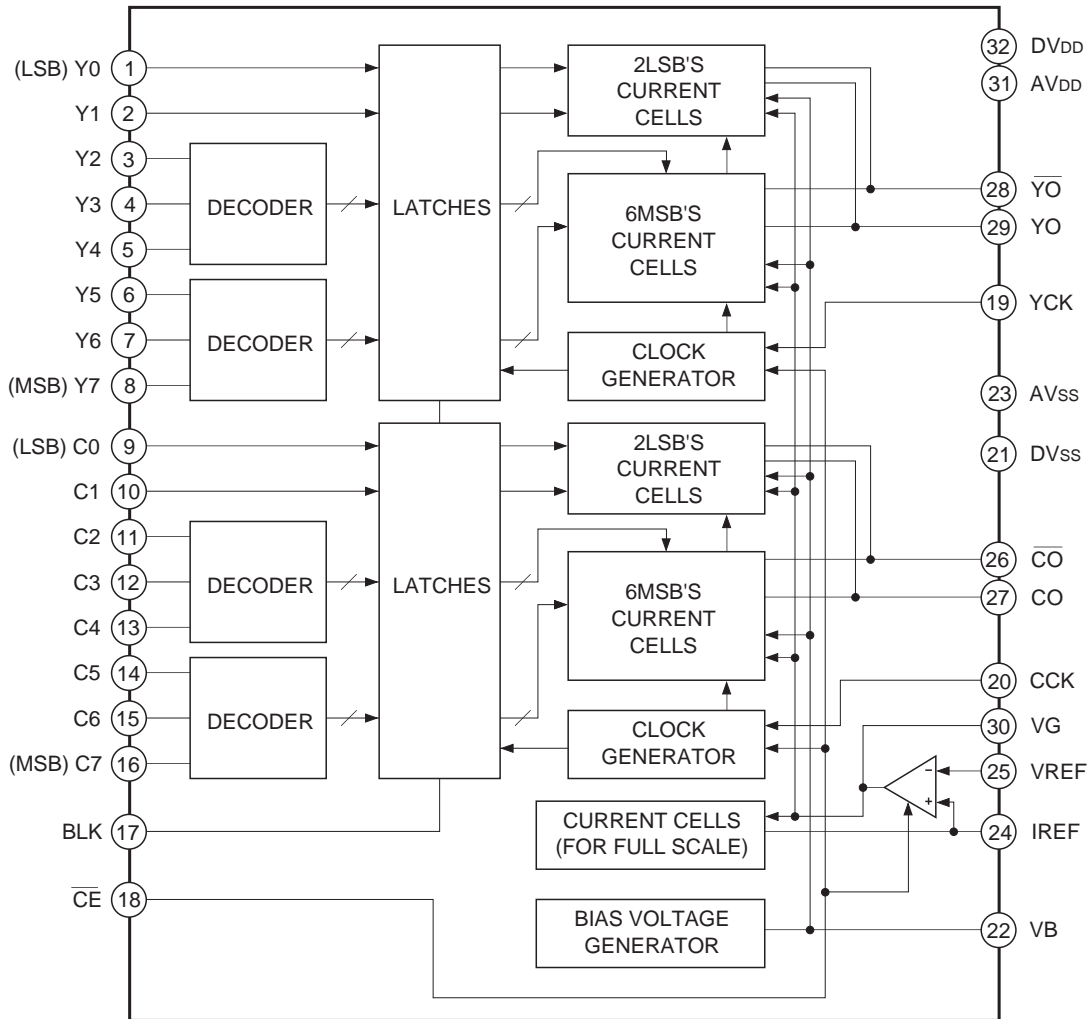
TPW1, TPW0	11.2 ns (min.) to 1.1 μ s (max.)
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- Operating temperature

ToPr	-40 to +85	°C
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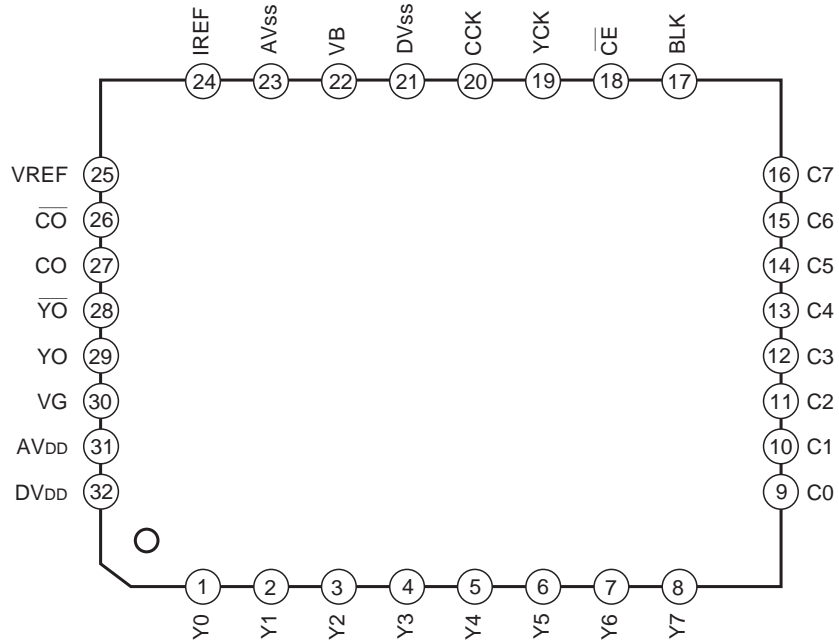
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Block Diagram



Pin Configuration



Pin Description and I/O Pins Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
1 to 8	Y0 to Y7	I		Digital input Y0 (LSB) to Y7 (MSB) C0 (LSB) to C7(MSB)
9 to 16	C0 to C7			
17	BLK	I		Blanking input. This is synchronized with the clock input signal for each channel. No signal at "H" (Output 0 V). Output condition at "L".
22	VB	O		Connect a capacitor of about 0.1 μF.
19	YCK	I		Clock input.
20	CCK			
21	DVss	—		Digital ground
23	AVss	—		Analog ground
18	$\overline{\text{CE}}$	I		Chip enable input. This is not synchronized with the clock input signal. No signal (Output 0 V) at "H" and minimizes power consumption.

Pin No.	Symbol	I/O	Equivalent circuit	Description
24	IREF	O		Connect a resistance 16 times "R _{IR} " that of output resistance value "R _{OUT} ".
25	VREF	I		Set full-scale output value.
30	VG	O		Connect a capacitor of about 0.1 μF.
31	AV _{DD}	—		Analog power supply
27	CO	O		Current output. Voltage output can be obtained by connecting a resistance.
29	YO			
26	$\overline{\text{CO}}$			Inverted current output. Normally dropped to analog ground.
28	$\overline{\text{YO}}$			
32	DV _{DD}	—		Digital power supply

Electrical Characteristics

(F_{CLK}=40 MHz, AV_{DD}=DV_{DD}=5 V, R_{OUT}=200 Ω, V_{REF}=2.0 V, Ta=25 °C)

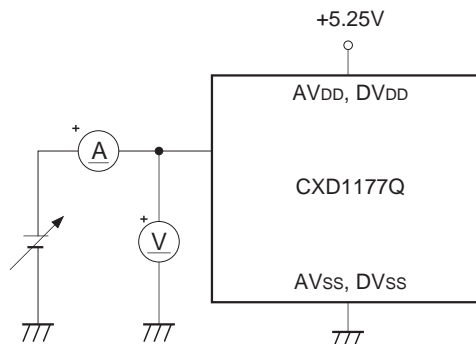
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			8		bit
Conversion speed	F _{CLK}	AV _{DD} =DV _{DD} =4.75 to 5.25 V Ta=-40 to +85 °C	0.5		40	MSPS
Integral non-linearity error	EL	Endpoint	-2.5		2.5	LSB
Differential non-linearity error	ED		-0.3		0.3	LSB
Output full-scale voltage	V _{FS}		1.8	2.0	2.2	V
Output full-scale ratio *1	F _{SR}		0	1.5	3.0	%
Output full-scale current	I _{FS}			10	15	mA
Output offset voltage	V _{OS}	When "00000000" data input			1	mV
Glitch energy	GE	R _{OUT} =75 Ω		30		pV*s
Crosstalk	CT	When 1 kHz sine wave input		57		dB
Supply current	I _{DD}	When 14.3 MHz color bar data input	C _E =L		32	mA
	I _{STB}		C _E =H		1.2	
Analog input resistance	R _{IN}	V _{REF}	1			MΩ
Input capacitance	C _I				9	pF
Digital input voltage	V _{IH}	AV _{DD} =DV _{DD} =4.75 to 5.25 V Ta=-20 to +75 °C	2.4			V
	V _{IL}				0.8	
Digital input current	I _{IH}	AV _{DD} =DV _{DD} =4.75 to 5.25 V Ta=-20 to +75 °C	-5		5	μA
	I _{IL}					
Setup time	t _s	R _{OUT} =75 Ω	5			ns
Hold time	t _h	R _{OUT} =75 Ω	10			ns
Propagation delay time	t _{PD}			10		ns
C _E enable time *2	t _E	C _E =H→L		2	4	ms
C _E disable time *2	t _D	C _E =L→H		2	4	ms

*1 Full-scale output ratio = $\left| \frac{\text{Full-scale voltage for each channel}}{\text{Full-scale voltage average value for each channels}} - 1 \right| \times 100 (\%)$

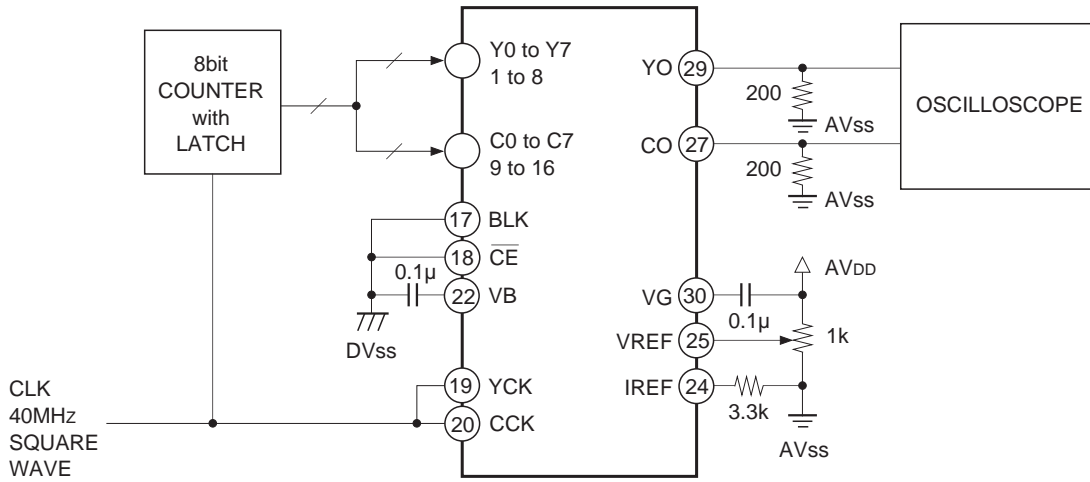
*2 When the external capacitors for the VG pins are 0.1 μF.

Electrical Characteristics Measurement Circuit

Analog Input Resistance } Measurement Circuit
 Digital Input Current }

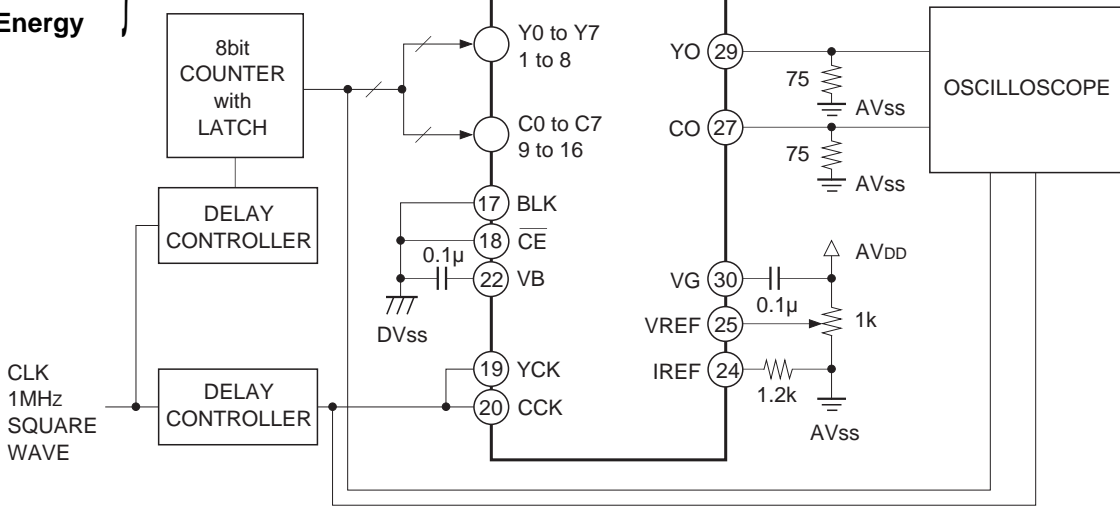


Maximum Conversion Velocity Measurement Circuit

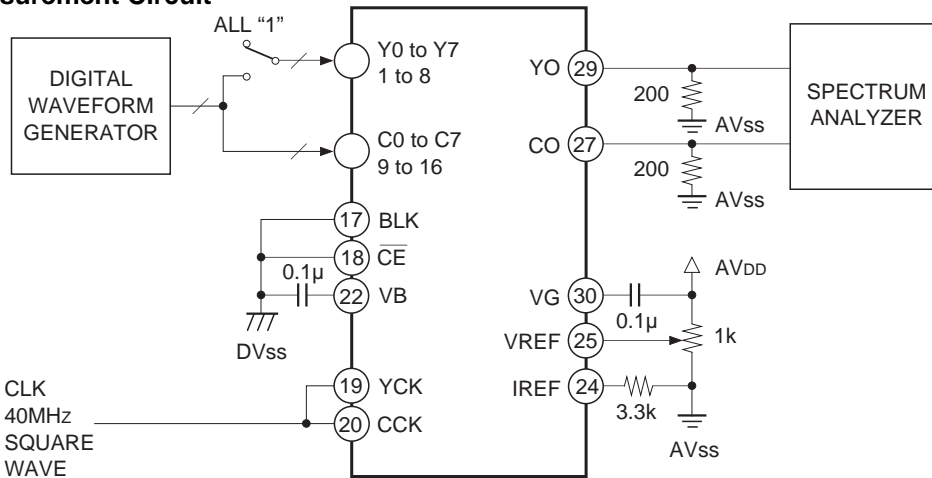


Setup Time
Hold Time
Glitch Energy

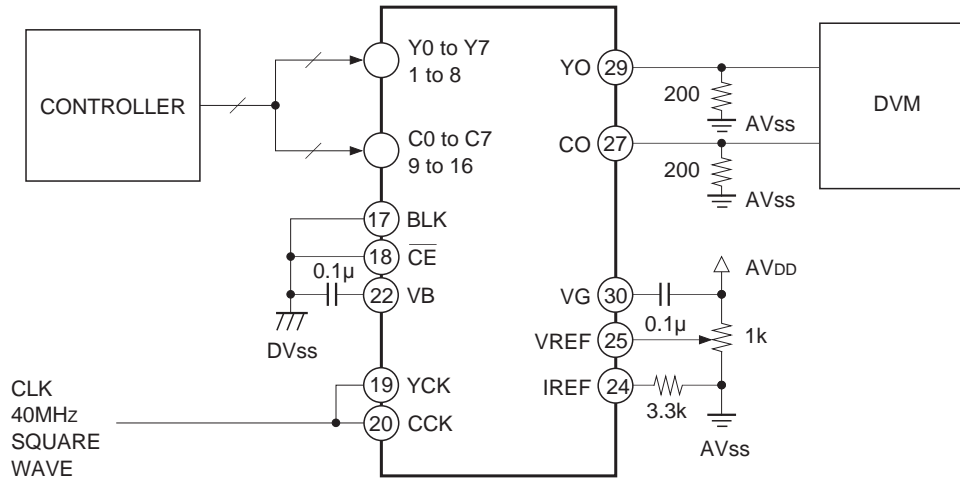
Measurement Circuit



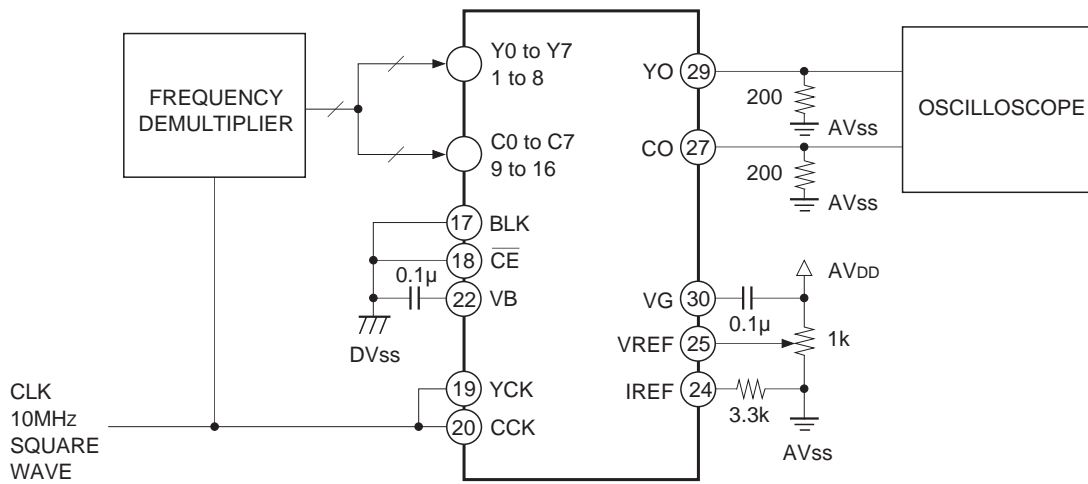
Crosstalk Measurement Circuit



DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit



Notes on Operation

- How to select the output resistance

The CXD1177Q is a D/A converter of the current output type. To obtain the output voltage connect the resistance to the current output pins Y0, C0. For specifications we have;

Output full scale voltage $V_{FS} = 1.8$ to 2.2 [V]

Output full scale current $I_{FS} =$ less than 15 [mA]

Calculate the output resistance value from the relation of $V_{FS} = I_{FS} \times R_{OUT}$. Also, 16 times resistance of the output resistance is connected to reference current pin IREF. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF} \times 16R_{OUT}/R_{IR}$. R_{OUT} is the resistance connected to the current output pins Y0 and C0 while R_{IR} is connected to IREF. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

- Phase relation between data and clock

To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the setup time (t_s) and hold time (t_H) as stipulated in the Electrical Characteristics.

- Power supply and grand

To reduce noise effects separate analog and digital systems in the device periphery. For the power supply pins, both digital and analog, bypass respective grounds by using a ceramic capacitor of about $0.1 \mu\text{F}$, as close as possible to the pin.

- Latch up

AV_{DD} and DV_{DD} have to be common at the PCB power supply source. This is to prevent latch up due to voltage difference between AV_{DD} and DV_{DD} pins when power supply is turned ON.

- $\overline{Y0}$ and $\overline{I0}$ pins

The $\overline{Y0}$ and $\overline{I0}$ pins are the inverted current output pins described in the Pin Description. The sums shown below become the constant value for any input data.

a) The sum of the currents output form Y0 and $\overline{Y0}$

b) The sum of the currents output form C0 and $\overline{C0}$

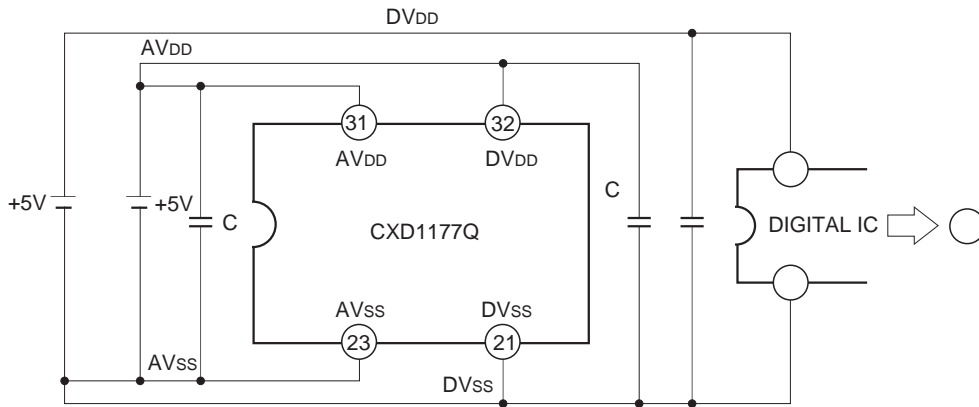
However, the performances such as the linearity error of the inverted current output pin output current is not guaranteed.

Latch Up Prevention

The CXD1177Q is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pin 31) and DV_{DD} (Pin 32), when power supply is ON.

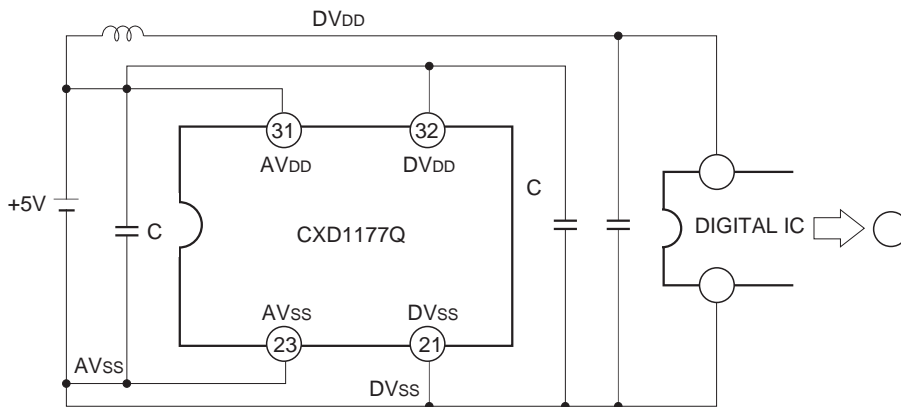
1. Correct usage

a. When analog and digital supplies are from different sources

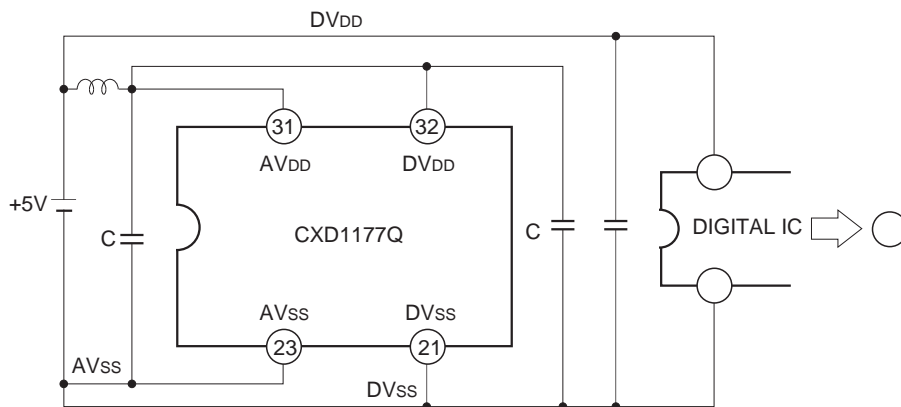


b. When analog and digital supplies are from a common source

(i)

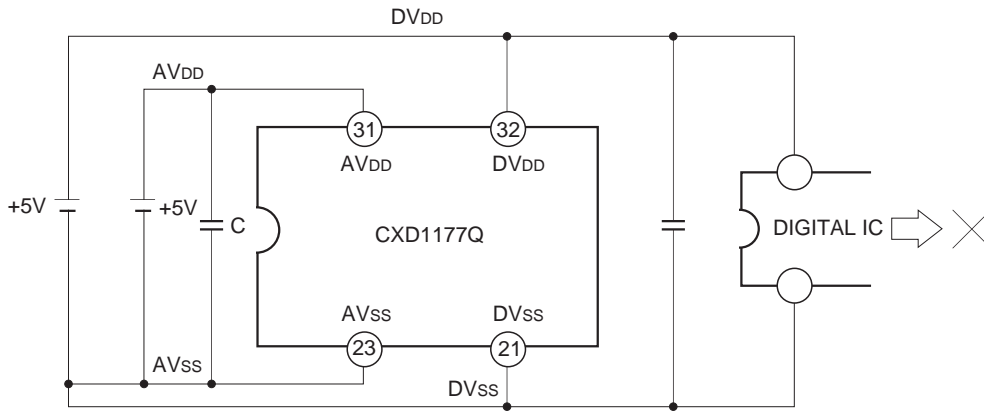


(ii)



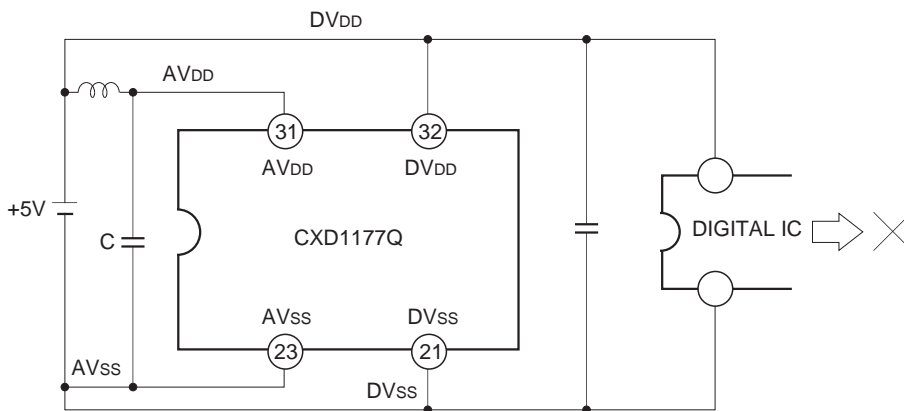
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

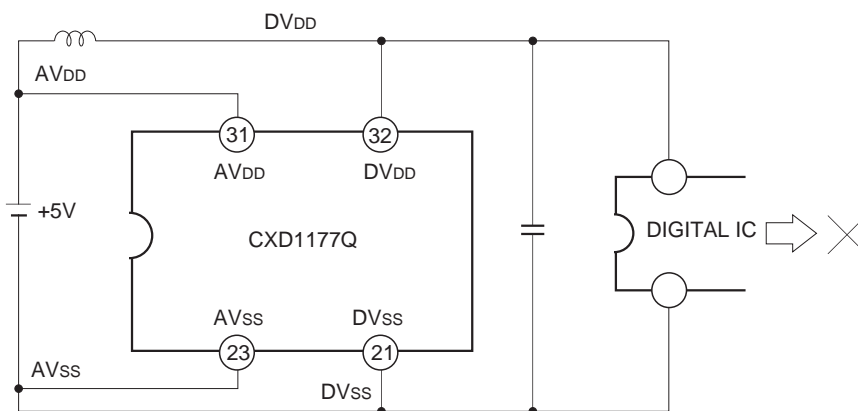


b. When analog and digital supplies are from common source

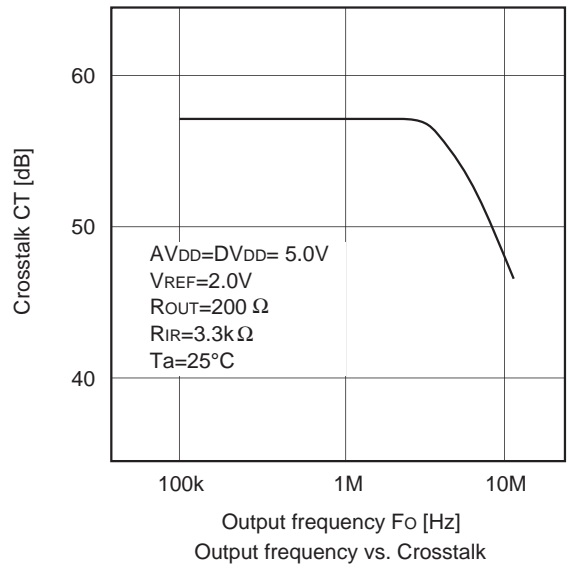
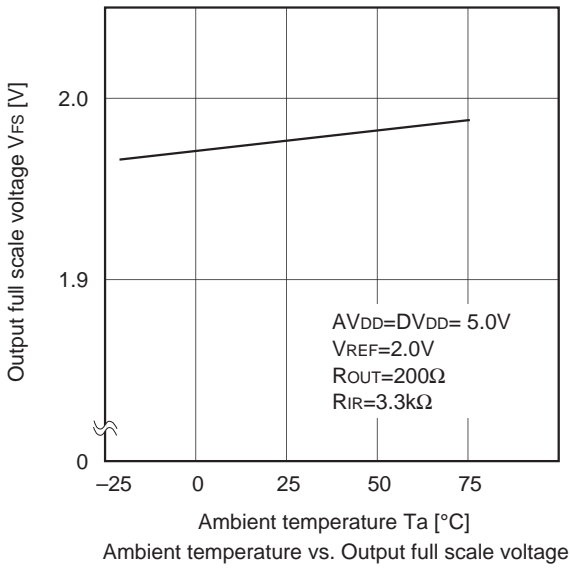
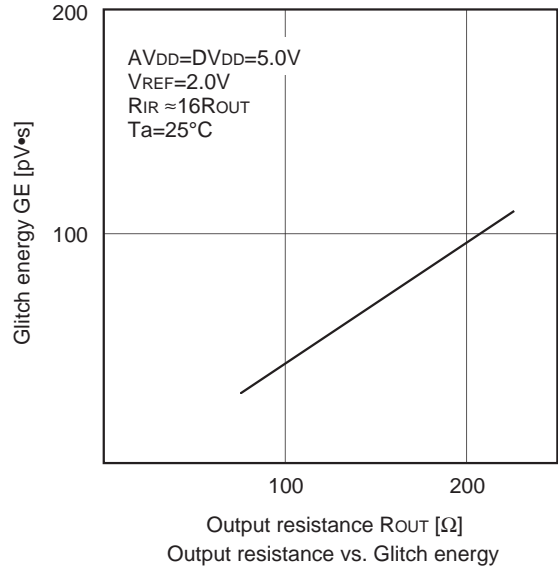
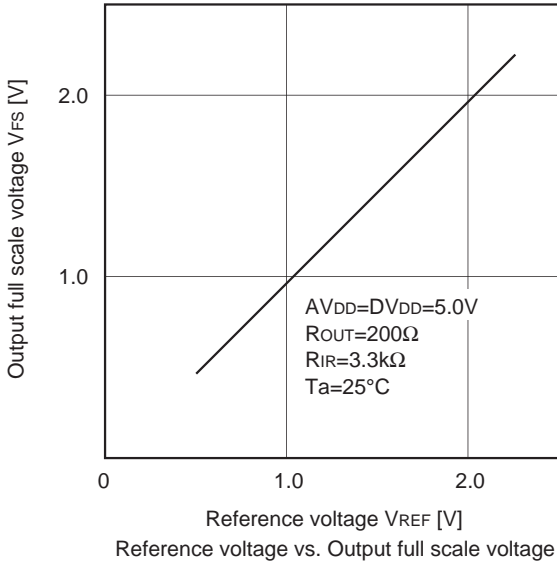
(i)



(ii)

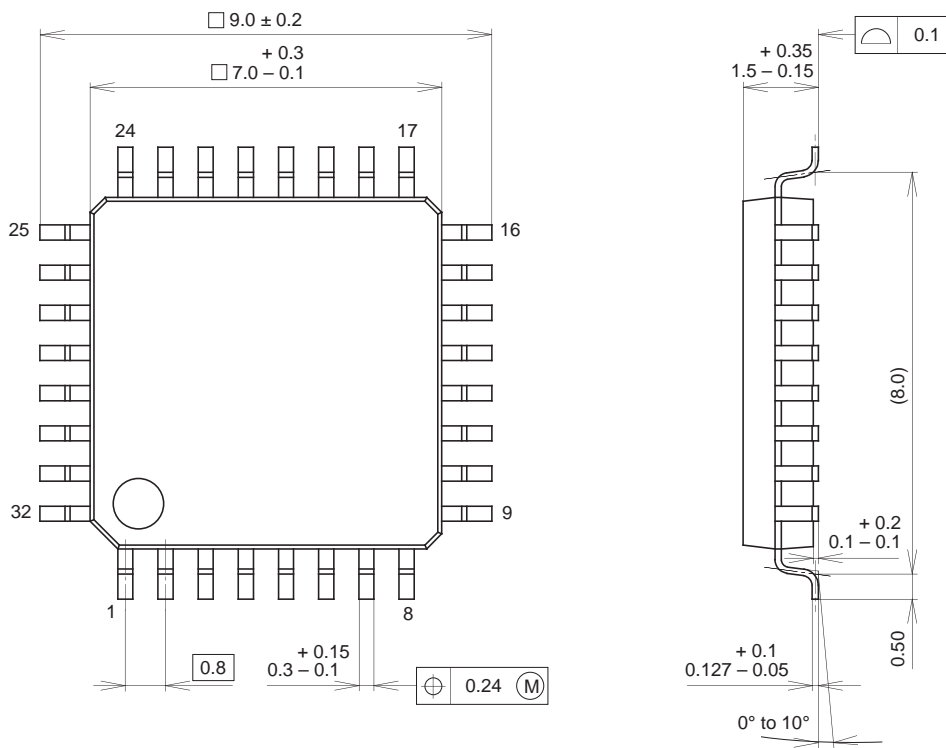


Example of Representative Characteristics



Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g