FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21363-2E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F72SP

■ DESCRIPTION

The Fujitsu MB15F72SP is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1300 MHz and a 350 MHz prescalers. A 64/65 or a 128/129 for the 1300 MHz prescaler, and a 8/9 or a 16/17 for the 350 MHz prescaler can be selected for the prescaler that enables pulse swallow operation.
MB15F72SP has the same configuration with MB15F02 or MB15F02L. The BiCMOS process is used , as a result a supply current is typically 2.7 mA typ. at 2.7 V.The supply voltage range is from 2.4 V to 3.6 V. A refined charge pump supplies well-balanced output current with 1.5 mA and 6 mA selectable by serial data.
The new package(BCC20) decreases a area of MB15F72SP more than 30 % comparing with the former BCC16 (for dual PLL).
MB15F72SP is ideally suited for wireless mobile communications, such as PDC

■ FEATURES

- High frequency operation:RF synthesizer: 1300 MHz max
  :IF synthesizer: 350 MHz max
- Low power supply voltage: V_{CC} = 2.4 to 3.6 V
- Ultra Low power supply current:I_{CC} = 2.7 mA typ. (V_{CC} = Vp = 2.7 V, SW_{IF} = SW_{RF} = 0, Ta = +25°C, in IF, RF locking state)
- Direct power saving function:Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 2.7 V, Ta = +25°C)
  Max. 10 µA (V_{CC} = Vp = 2.7 V)

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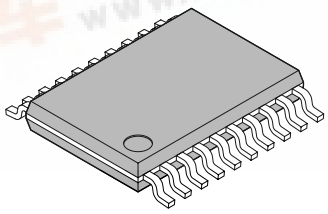
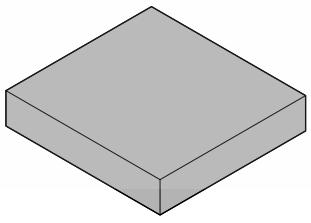
■ PACKAGES

20-pin plastic TSSOP



(FPT-20P-M06)

20-pad plastic BCC



(LCC-20P-M04)

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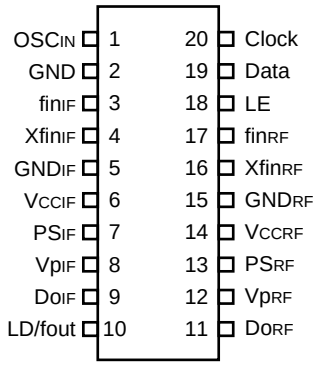
- Software selectable charge pump current: 1.5 mA/6.0 mA (typ.)
- Dual modulus prescaler: 1300 MHz prescaler (64/65 or 128/129)/350 MHz prescaler (8/9 or 16/17)
- 23 bit shift resister
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- On–chip phase control for phase comparator
- Built-in digital locking detector circuit to detect PLL locking and unlocking.
- Operating temperature: Ta = –40°C to +85°C
- Sireal data format compatible with MB15F02SL
- Small package BCC20 (3.4 mm × 3.6mm × 0.8mm)

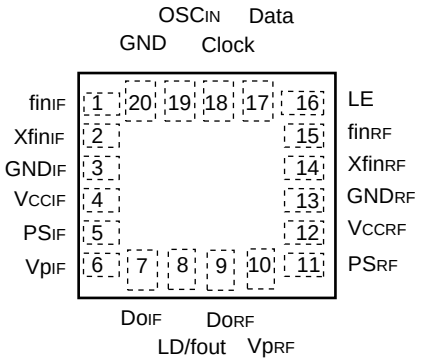
■ PIN ASSIGNMENTS

(TSSOP-20)
TOP VIEW



(FPT-20P-M06)

(BCC-20)
TOP VIEW

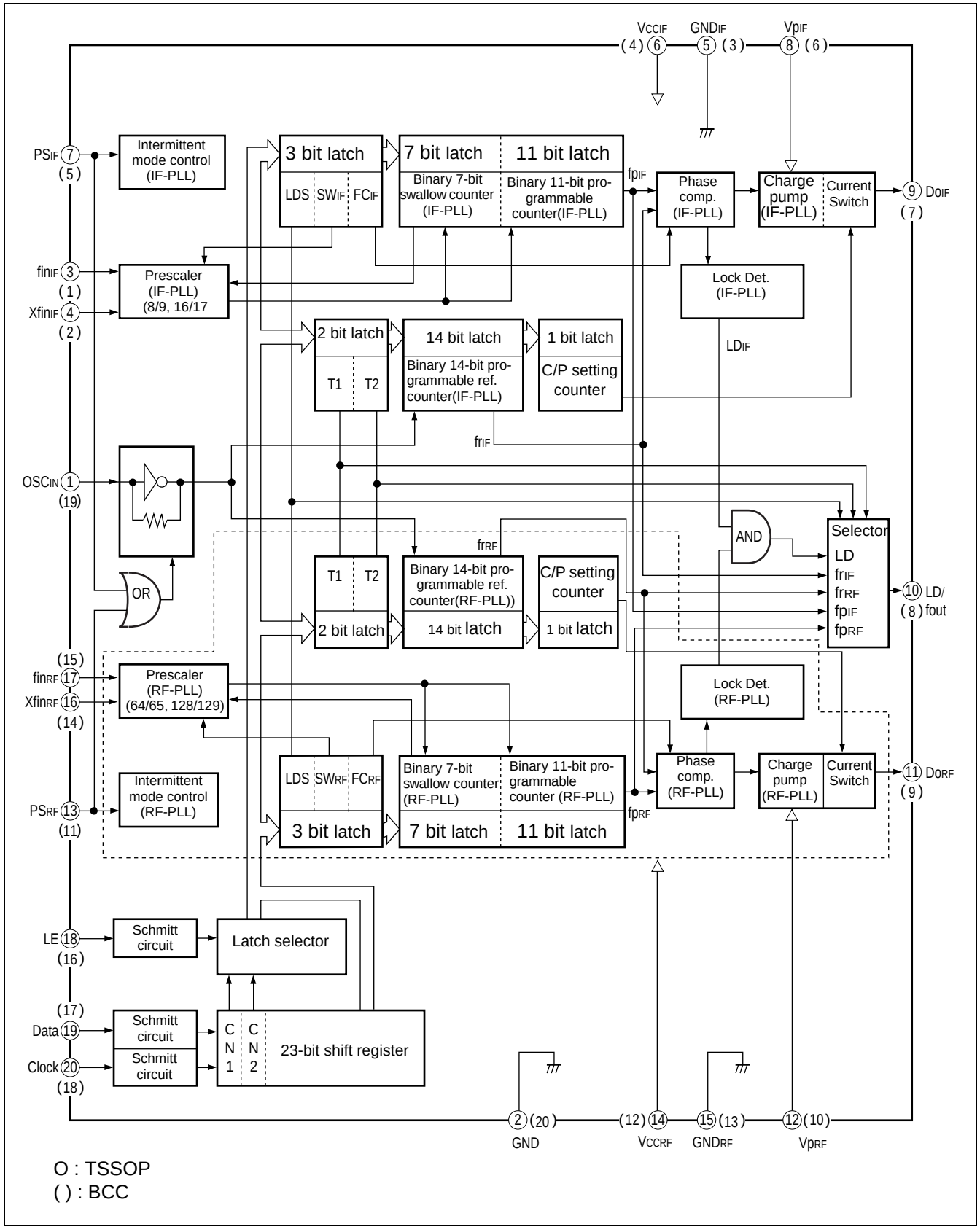


(LCC-20P-M04)

■ PIN DESCRIPTION

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC_{IN}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
2	20	GND	—	Ground for OSC input buffer and the shift register circuit.
3	1	fin_{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be via AC coupling.
4	2	$Xfin_{IF}$	I	Prescaler complimentary input pin for the IF-PLL section. This pin should be grounded via a capacitor.
5	3	GND_{IF}	—	Ground for the IF-PLL section.
6	4	V_{CCIF}	—	Power supply voltage input pin for the IF-PLL section(except for the charge pump circuit), the OSC input buffer and the shift register circuit. When power is OFF, latched data of IF-PLL is lost.
7	5	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.) PS_{IF} = “H” ; Normal mode / PS_{IF} = “L” ; Power saving mode
8	6	Vp_{IF}	—	Power supply voltage input pin for the IF-PLL charge pump.
9	7	D_{OIF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FCbit.
10	8	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout).The output signal is selected by LDS bit in the serial data. LDS bit = “H” ; outputs fout signal / LDS bit = “L” ; outputs LD signal
11	9	D_{ORF}	O	Charge pump output for the RF-PLL section. Phase characterstics of the phase detector can be reversed by FCbitt.
12	10	Vp_{RF}	—	Power supply voltage input pin for the RF-PLL charge pump.
13	11	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at “L” Power-ON. (Open is prohibited.) PS_{RF} = “H” ; Normal mode / PS_{RF} = “L” ; Power saving mode
14	12	V_{CCRF}	—	Power supply voltage input pin for the RF-PLL section (except for the charge pump circuit).
15	13	GND_{RF}	—	Ground for the RF-PLL section.
16	14	$Xfin_{RF}$	I	Prescaler complimentary input pin for the RF-PLL section. This pin should be grounded via a capacitor.
17	15	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connection to an external VCO should be via AC coupling.
18	16	LE	I	Load enable signal input(with the schmitt trigger circuit). When LE is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input(with the schmitt trigger circuit). A data is transferred to the corresponding latch(IF-ref. counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit). One bit of data is shifted into the shift register on a rising edge of the clock.

■ BLOCK DIAGRAM



O : TSSOP
( ) : BCC

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage		V_{CC}	–0.5	4.0	V
		Vp	V_{CC}	4.0	V
Input voltage		V_I	–0.5	V_{CC} + 0.5	V
Output voltage	LD/fout	V_O	GND	V_{CC}	V
	Do_{IF}, Do_{RF}	V_{DO}	GND	Vp	V
Storage temperature		Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	2.7	3.6	V	$V_{CCRF} = V_{CCIF}$
	Vp	V_{CC}	2.7	3.6	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	–40	—	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCIF} *1	IF PLL	—	1.1	—	mA
		I_{CCRF} *2	RF PLL	—	1.6	—	mA
Power saving current		I_{PSIF}	PS_{IF} = PS_{RF} = "L"	—	0.1 *8	10	µA
		I_{PSRF}	PS_{IF} = PS_{RF} = "L"	—	0.1 *8	10	µA
Operating frequency	fin_{IF} *3	fin_{IF}	IF PLL	50	—	350	MHz
	fin_{RF} *3	fin_{RF}	RF PLL	100	—	1300	MHz
	OSC_{IN}	f_{OSC}	—	3	—	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	–15	—	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	–15	—	+2	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	V_{CC}	V_{P-P}
"H" level input voltage	Data, LE, Clock	V_{IH}	Schmitt trigger input	0.7 V_{CC} + 0.4	—	—	V
"L" level input voltage		V_{IL}	Schmitt trigger input	—	—	0.3 V_{CC} – 0.4	V
"H" level input voltage	PS_{IF}, PS_{RF}	V_{IH}	—	0.7 V_{CC}	—	—	V
"L" level input voltage		V_{IL}	—	—	—	0.3 V_{CC}	V
"H" level input current	Data, LE, Clock, PS_{IF}, PS_{RF}	I_{IH} *4	—	–1.0	—	+1.0	µA
"L" level input current		I_{IL} *4	—	–1.0	—	+1.0	µA
"H" level input current	OSC_{IN}	I_{IH}	—	0	—	+100	µA
"L" level input current		I_{IL} *4	—	–100	—	0	µA
"H" level output voltage	LD/fout	V_{OH}	V_{CC} = Vp = 2.7 V, I_{OH} = –1 mA	V_{CC} – 0.4	—	—	V
"L" level output voltage		V_{OL}	V_{CC} = Vp = 2.7 V, I_{OL} = 1 mA	—	—	0.4	V
"H" level output voltage	Do_{IF}, Do_{RF}	V_{DOH}	V_{CC} = Vp = 2.7 V, I_{DOH} = –0.5 mA	Vp – 0.4	—	—	V
"L" level output voltage		V_{DOL}	V_{CC} = Vp = 2.7 V, I_{DOL} = 0.5 mA	—	—	0.4	V
High impedance cutoff current	Do_{IF}, Do_{RF}	I_{OFF}	V_{CC} = Vp = 2.7 V, V_{OFF} = 0.5 V to Vp – 0.5 V	—	—	2.5	nA
"H" level output current	LD/fout	I_{OH} *4	V_{CC} = Vp = 2.7 V	—	—	–1.0	mA
"L" level output current		I_{OL}	V_{CC} = Vp = 2.7 V	1.0	—	—	mA

(Continued)

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(V_{CC} = 2.4 V to 3.6 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H" level output current	DO_{IF} DO_{RF}	I_{DOH} *4	V_{CC} = Vp = 2.7 V, V_{DOH} = Vp/2, Ta = +25 °C	CS bit = "H"	—	–6.0	—	mA
				CS bit = "L"	—	–1.5	—	mA
"L" level output current	DO_{IF} DO_{RF}	I_{DOL}	V_{CC} = Vp = 2.7 V, V_{DOL} = Vp/2, Ta = +25 °C	CS bit = "H"	—	6.0	—	mA
				CS bit = "L"	—	1.5	—	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = Vp / 2		—	3	—	%
	vs. V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ Vp – 0.5 V		—	10	—	%
	vs.Ta	I_{DOTA} *7	–40 °C ≤ Ta ≤ +85 °C, V_{DO} = Vp / 2		—	10	—	%

*1 : fin_{IF} = 270 MHz, fosc = 12.8 MHz, V_{CCIF} = Vp_{IF} = 2.7 V, SW_{IF} = 0, Ta = +25°C, in locking state.

*2 : fin_{RF} = 910 MHz, fosc = 12.8 MHz, V_{CCRF} = Vp_{RF} = 2.7 V, SW_{RF} = 0, Ta = +25°C, in locking state.

*3 : AC coupling. 1000pF capacitor is connected under the condition of min. operating frequency.

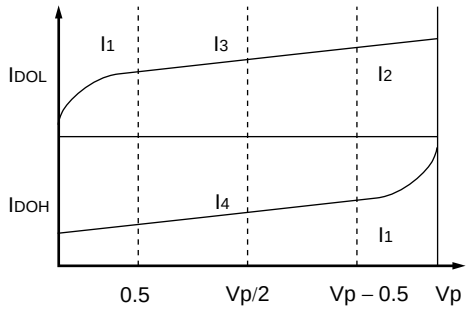
*4 : The symbol "–" (minus) means direction of current flow.

*5 : V_{CC} = Vp = 2.7 V, Ta = +25°C
$(||I_3| – |I_4||)/[(|I_3| + |I_4|)/2] \times 100(\%)$

*6 : V_{CC} = Vp = 2.7 V, Ta = +25°C (Applied to each I_{DOL}, I_{DOH})
$[(||I_2| – |I_1||)/2]/[(|I_1| + |I_2|)/2] \times 100(\%)$

*7 : V_{CC} = Vp = 2.7 V, Ta = +25°C (Applied to each I_{DOL}, I_{DOH})
$[||I_{DO(+85°C)}| – |I_{DO(–40°C)}||/2]/[|I_{DO(+85°C)}| + |I_{DO(–40°C)}|/2] \times 100(\%)$

*8 : fosc = 12.8 MHz, V_{CCRF} = Vp_{RF} = V_{CCIF} = 2.7 V, Ta = +25°C



Charge pump output voltage (V)

■ FUNCTIONAL DESCRIPTION

1. Pulse swallow function :

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (8 or 16 for IF-PLL, 64 or 128 for RF-PLL)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC} : Reference oscillation frequency (OSC_{IN} input frequency)
R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

2. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, and programmable reference dividers of IF/RF-PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On a rising edge of Clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

	The programmable reference counter for the IF-PLL	The programmable reference counter for the RF-PLL	The programmable counter and the swallow counter for the IF-PLL	The programmable counter and the swallow counter for the RF-PLL
CN1	0	1	0	1
CN2	0	0	1	1

(1) Shift Register Configuration

- **Programmable Reference Counter**

(LSB) Data Flow → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CS : Charge pump currnet select bit
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383)
T1, T2 : Test purpose bit
CN1, CN2 : Control bit
X : Dummy bits (Set “0” or “1”)

Note : Data input with MSB first.

• **Programmable Counter**

(LSB) Data Flow → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW_{IF}/ SW_{RF}	FC_{IF}/ FC_{RF}	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127)
N1 to N11 : Divide ratio setting bits for the programmable counter (3 to 2,047)
LDS : LD/fout signal select bit
SW_{IF}/SW_{RF} : Divide ratio setting bit for the prescaler (IF : SW_{IF},RF : SW_{RF})
FC_{IF}/FC_{RF} : Phase control bit for the phase detector (IF: FC_{IF}, RF: FC_{RF})
CN1, CN2 : Control bit

Note**:** Data input with MSB first.

(2) Data setting

• Binary 14-bit Programmable Reference Counter Data Setting (R1 to R14)

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 11-bit Programmable Counter Data Setting (N1 to N11)

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note : Divide ratio less than 3 is prohibited.

• Binary 7-bit Swallow Counter Data Setting (A1 to A7)

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

- Prescaler Data Setting (SW)

Divide ratio	SW = "1"	SW = "0"
Prescaler divide ratio IF-PLL	8/9	16/17
Prescaler divide ratio RF-PLL	64/65	128/129

- Charge Pump Current Setting (CS)

Current value	CS
±6.0 mA	1
±1.5 mA	0

- LD/fout Output Select Data Setting (LDS)

LD/fout output signal	LDS
fout signal	1
LD signal	0

- Test Purpose Bit Setting (T1, T2)

LD/fout pin state	T1	T2
Outputs fr_{IF}.	0	0
Outputs fr_{RF}.	1	0
Outputs fp_{IF}.	0	1
Outputs fp_{RF}.	1	1

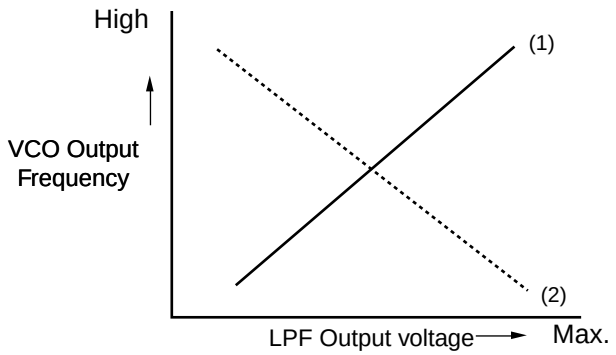
- Phase Comparator Phase Switching Data Setting (FC_{IF}, FC_{RF})

Phase comparator input	FC_{IF} = "1"	FC_{RF} = "1"	FC_{IF} = "0"	FC_{RF} = "0"
	DO_{IF}	DO_{RF}	DO_{IF}	DO_{RF}
fr > fp	H		L	
fr < fp	L		H	
fr = fp	Z		Z	

Z : High-impedance

Depending upon the VCO and LPF polarity, FC bit should be set.

(1) VCO polarity FC = "1"
(2) VCO polarity FC = "0"



Note : Give attention to the polarity for using active type LPF.

3. Power Saving Mode (Intermittent Mode Control Circuit)

Status	PS_{IF}/PS_{RF} pins
Normal mode	H
Power saving mode	L

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pins low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

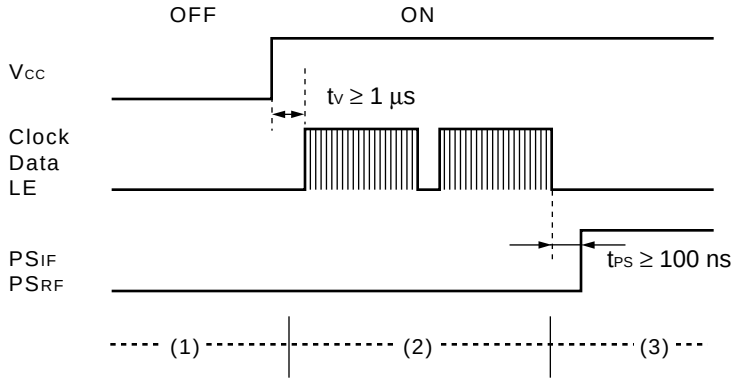
Setting the PS pins high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes •When power (V_{CC}) is first applied, the device must be in standby mode, PS_{IF} = PS_{RF} = Low, for at least 1 µs.

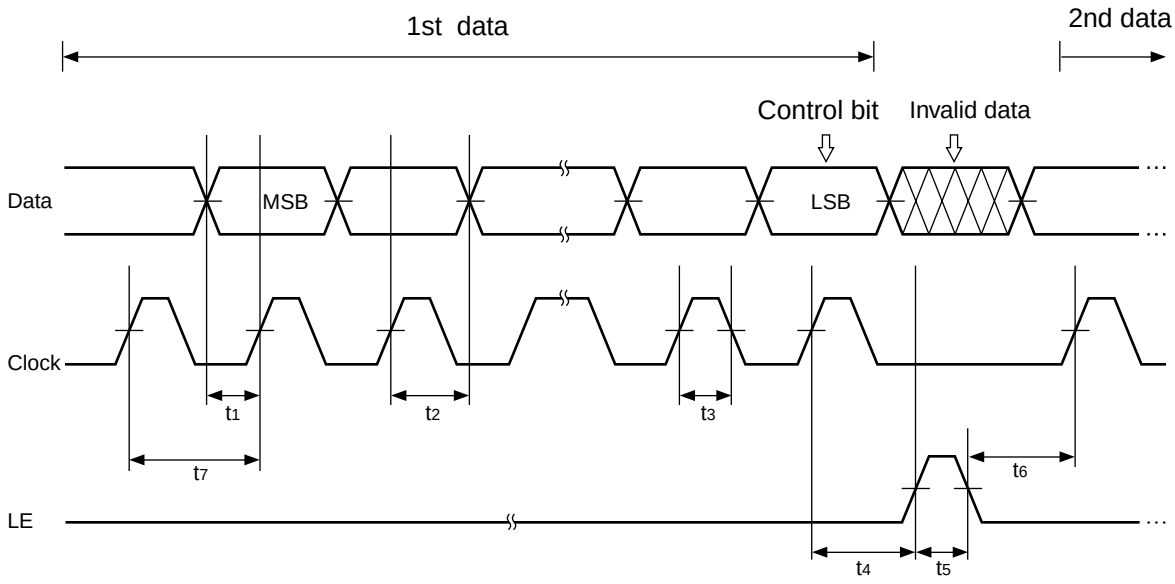
•PS pins must be set at “L” for Power-ON.



(1) PS_{IF} = PS_{RF} = “L” (power saving mode) at Power-ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V).
(3) Release power saving mode (PS_{IF}, PS_{RF} : “L” → “H”) 100 ns later after setting serial data.

4. SERIAL DATA INPUT TIMING

Frequency multiplier setting is performed through a serial interface using the Data pin, Clock pin, and LE pin. Setting data is read into the shift register at the rise of the clock signal, and transferred to a latch at the rise of the LE signal. The following diagram shows the data input timing.

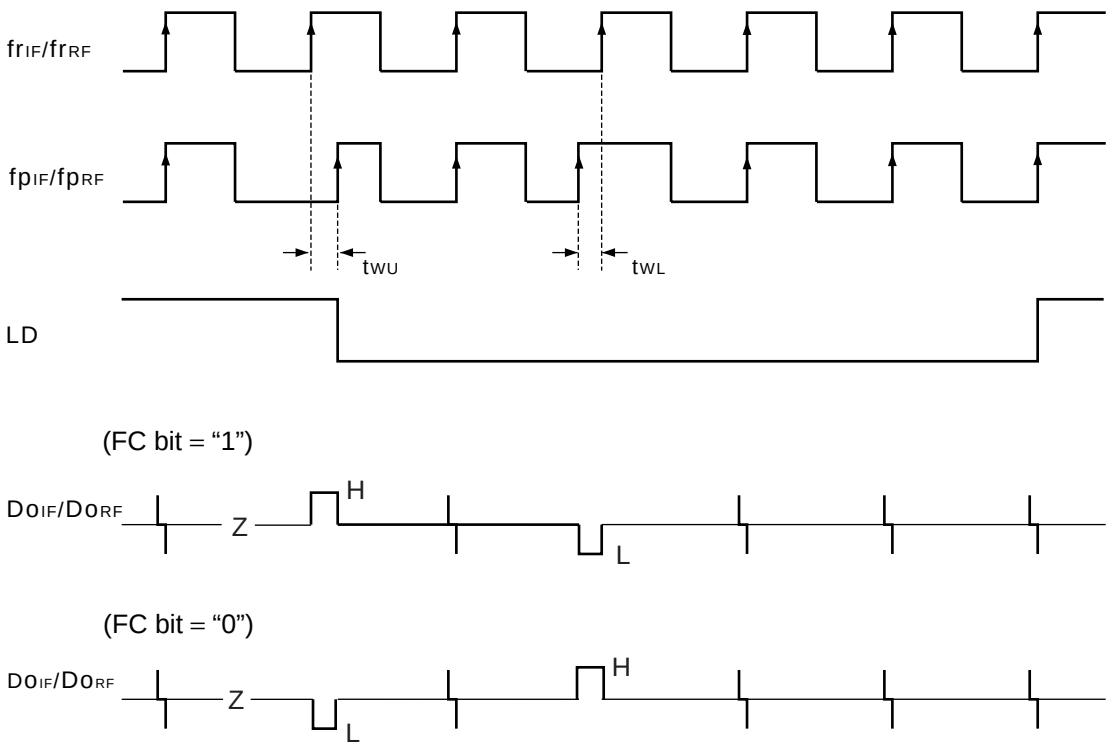


Parameter	Min.	Typ.	Max.	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note : LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



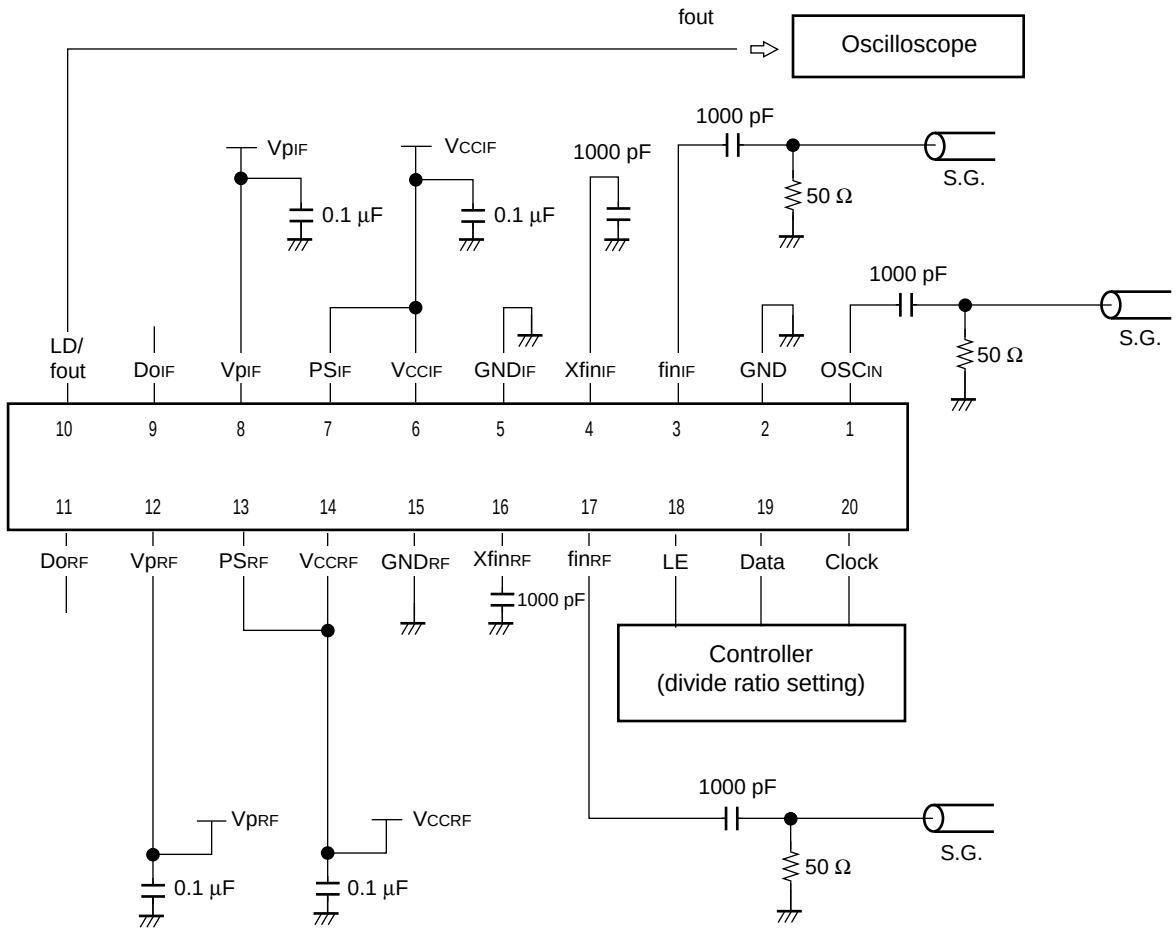
• LD Output Logic

IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes: •Phase error detection range = -2π to $+2\pi$

- Pulses on Do_{IF}/Do_{RF} signals are output to prevent dead zone during locking state.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
  $t_{WU} \geq 2/fosc$: e.g. $t_{WU} \geq 156.3$ ns when fosc = 12.8 MHz
  $t_{WU} \leq 4/fosc$: e.g. $t_{WL} \leq 312.5$ ns when fosc = 12.8 MHz

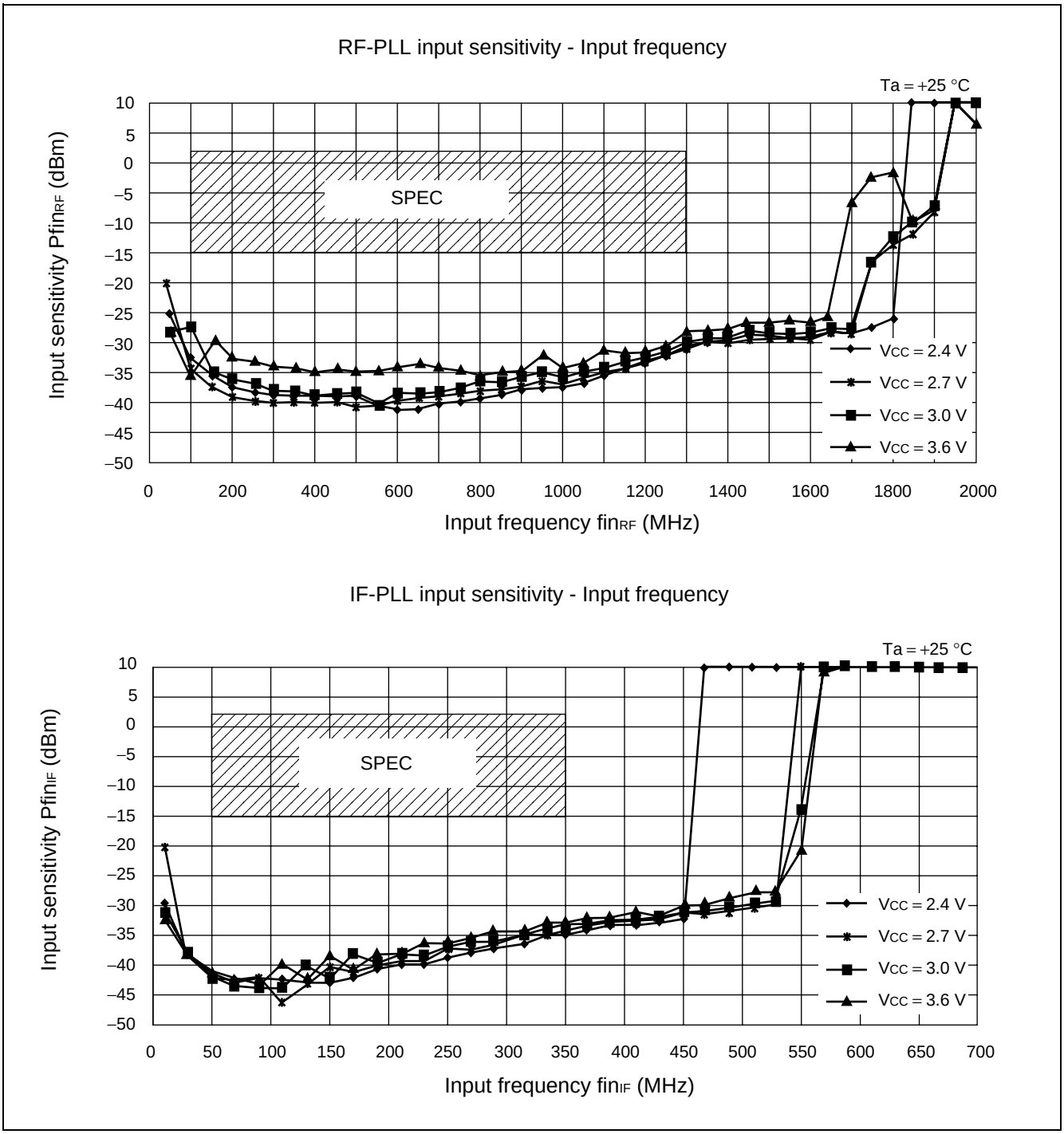
■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



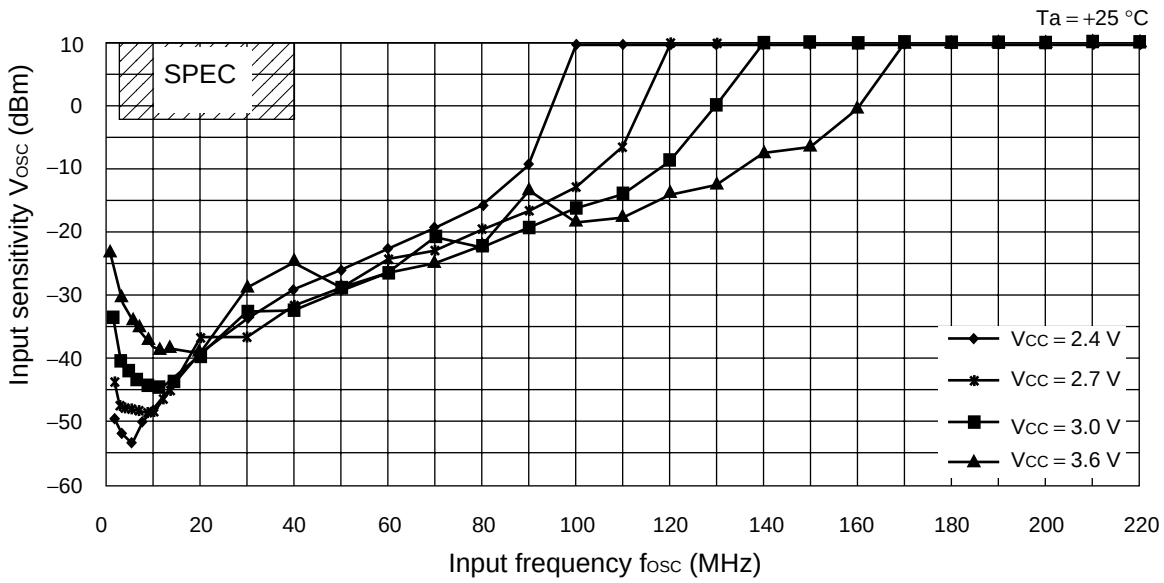
Note : Terminal number shows that of TSSOP-20.

■ TYPICAL CHARACTERISTICS

1. fin input sensitivity



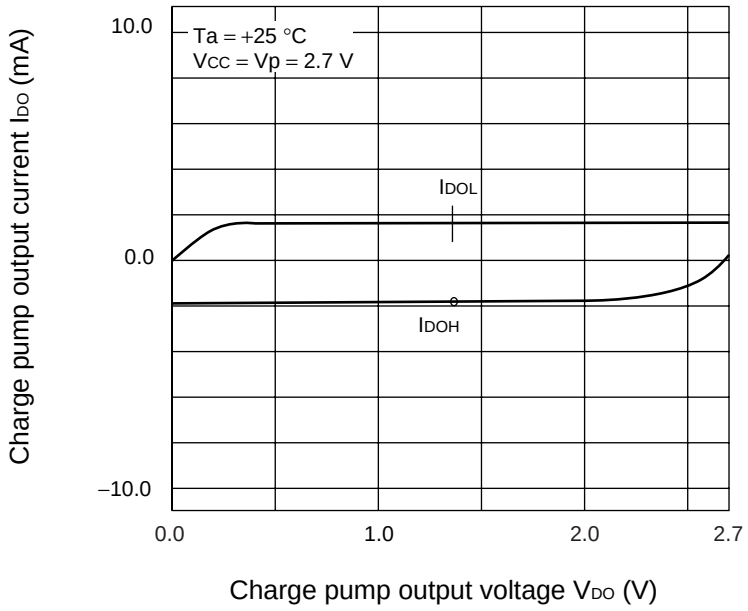
2. OSC_{IN} input sensitivity



3. RF-PLL Do output current

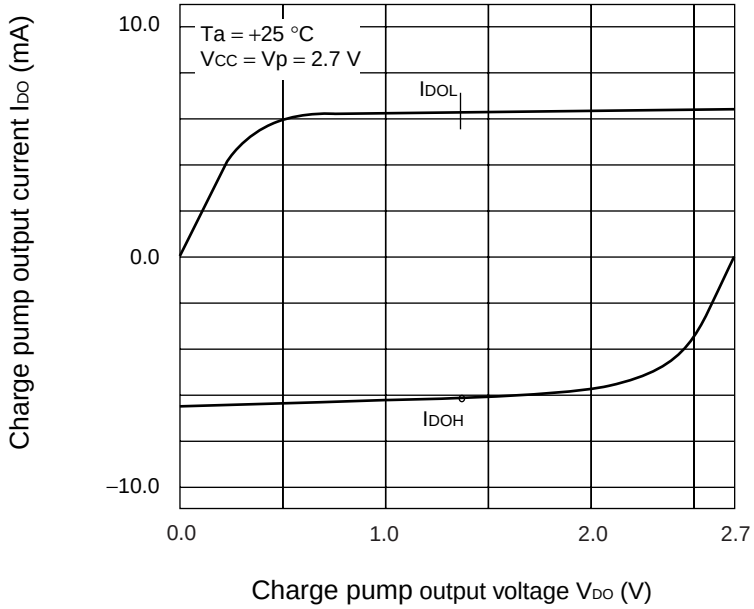
- 1.5 mA mode

I_{DO} - V_{DO}



- 6.0 mA mode

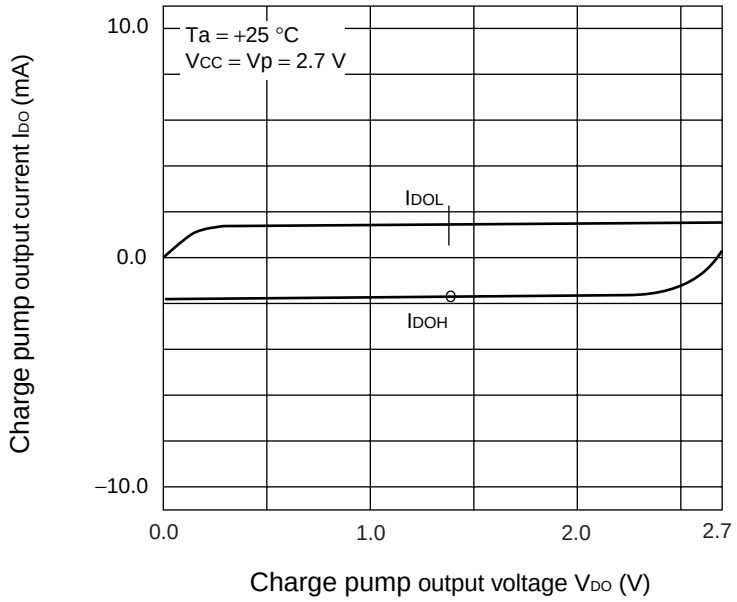
I_{DO} - V_{DO}



4. IF-PLL Do output current

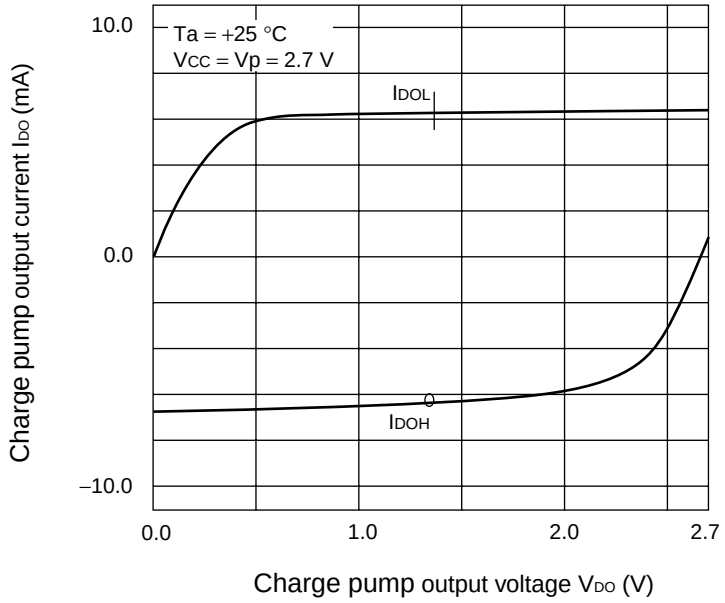
- 1.5 mA mode

$I_{DO} - V_{DO}$



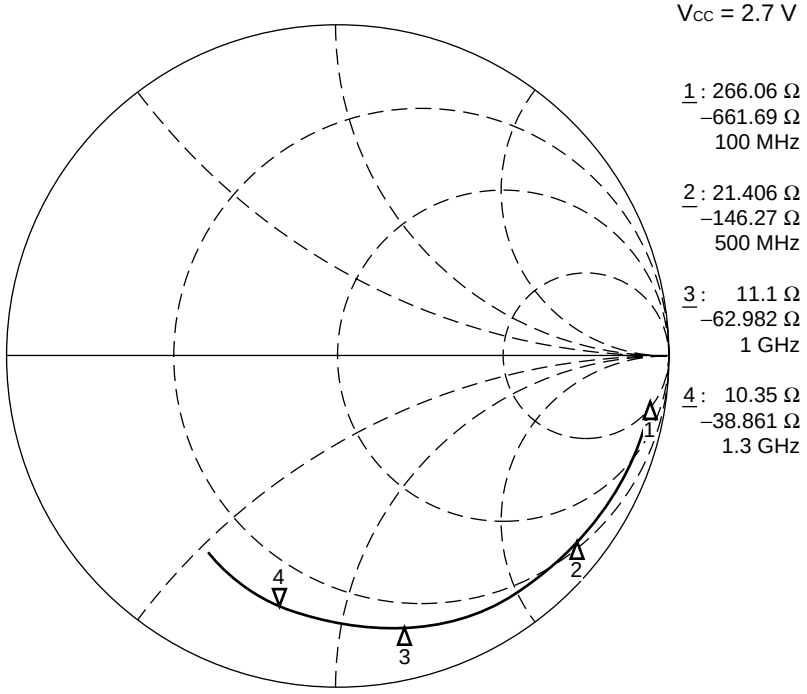
- 6.0 mA mode

$I_{DO} - V_{DO}$

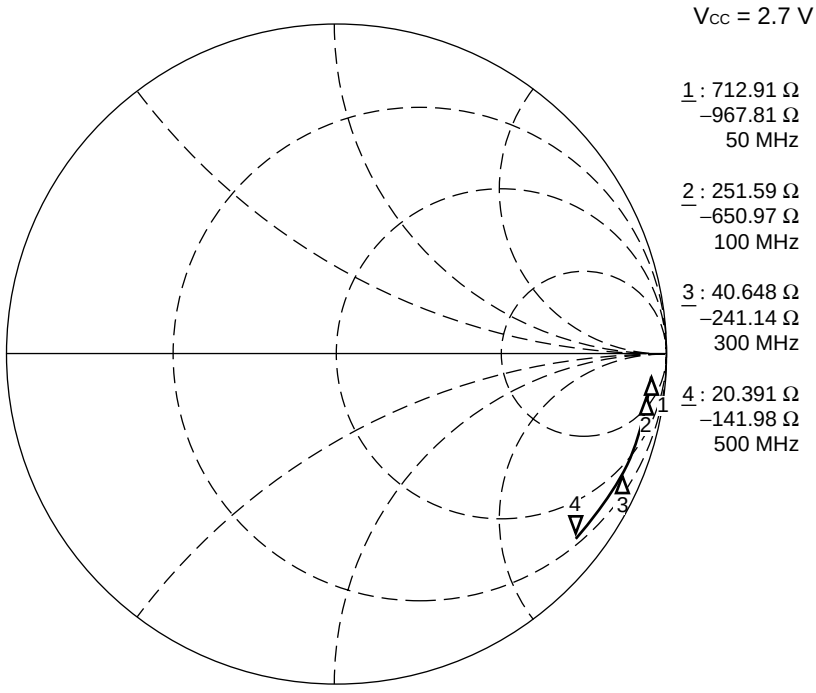


5. fin input impedance

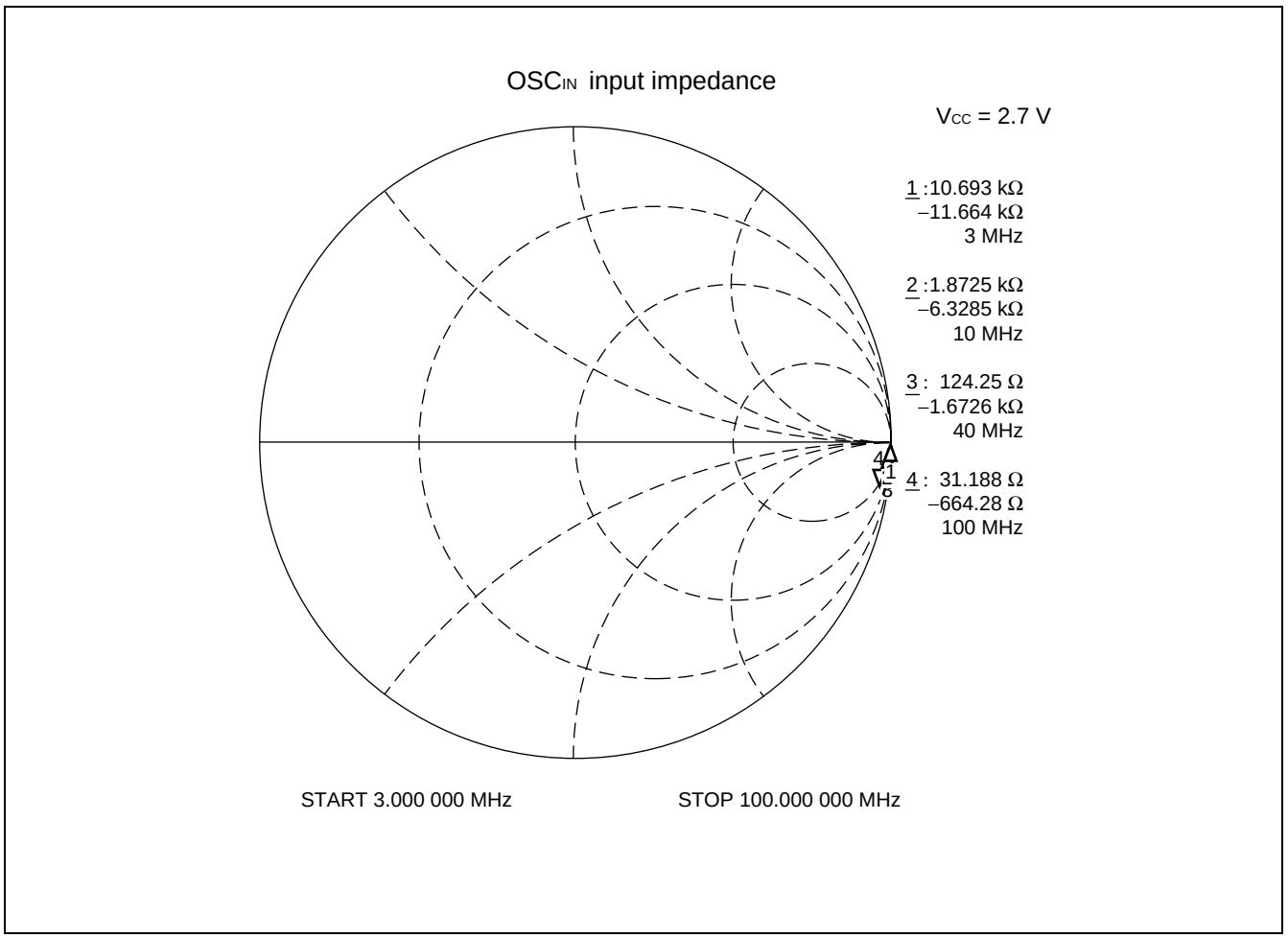
finRF input impedance



finIF input impedance

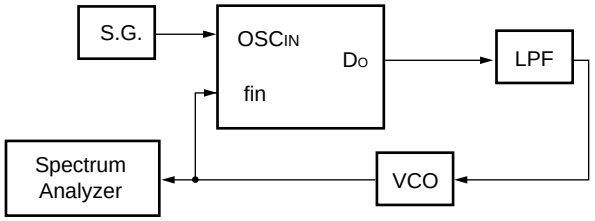


6. OSC_{IN} input impedance



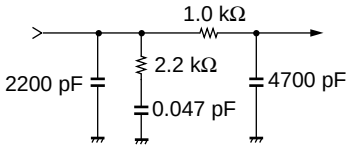
■ REFERENCE INFORMATION
(for Lock-up Time, Phase Noise and Reference Leakage)

Test Circuit

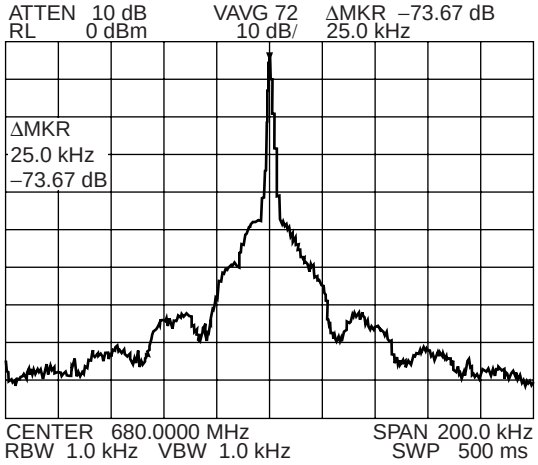


f_{VCO} = 680 MHz
K_V = 50 MHz/V
fr = 25 kHz
f_{OSC} = 14.4 MHz
LPF

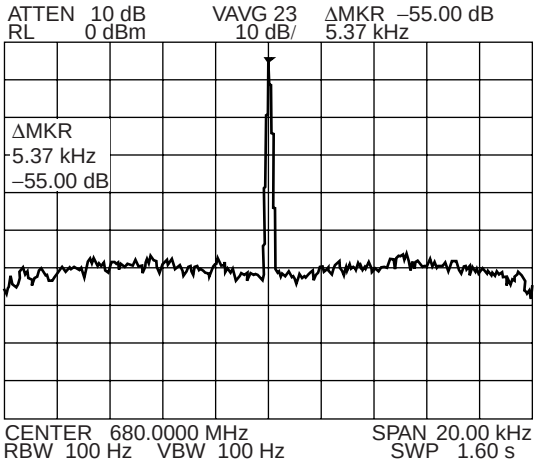
V_{CC} = 3.0 V
V_{VCO} = 2.2 V
Ta = + 25 °C
CP : 6 mA mode



- PLL Reference Leakage



- PLL Phase Noise

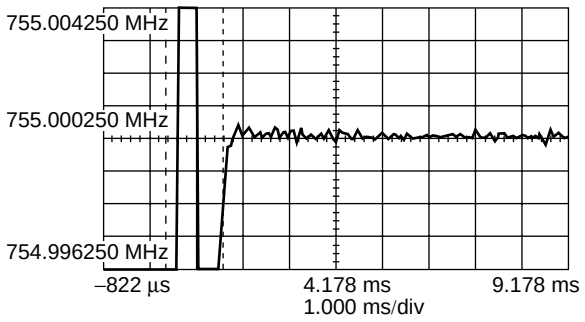


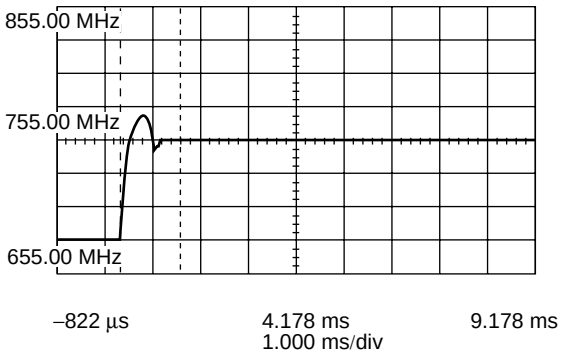
(Continued)

(Continued)

• PLL Lock Up time

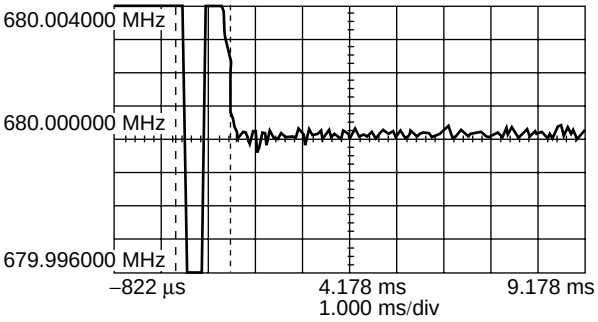
680 MHz→755 MHz within±1 kHz
Lch→Hch 1.244 ms

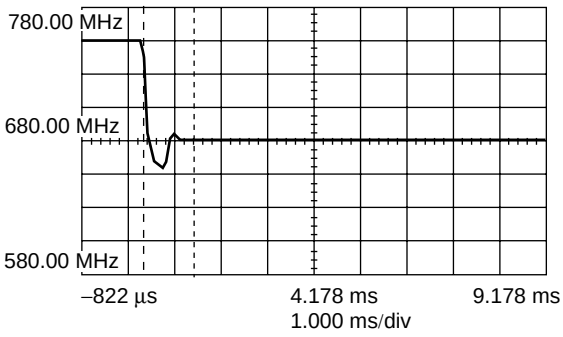




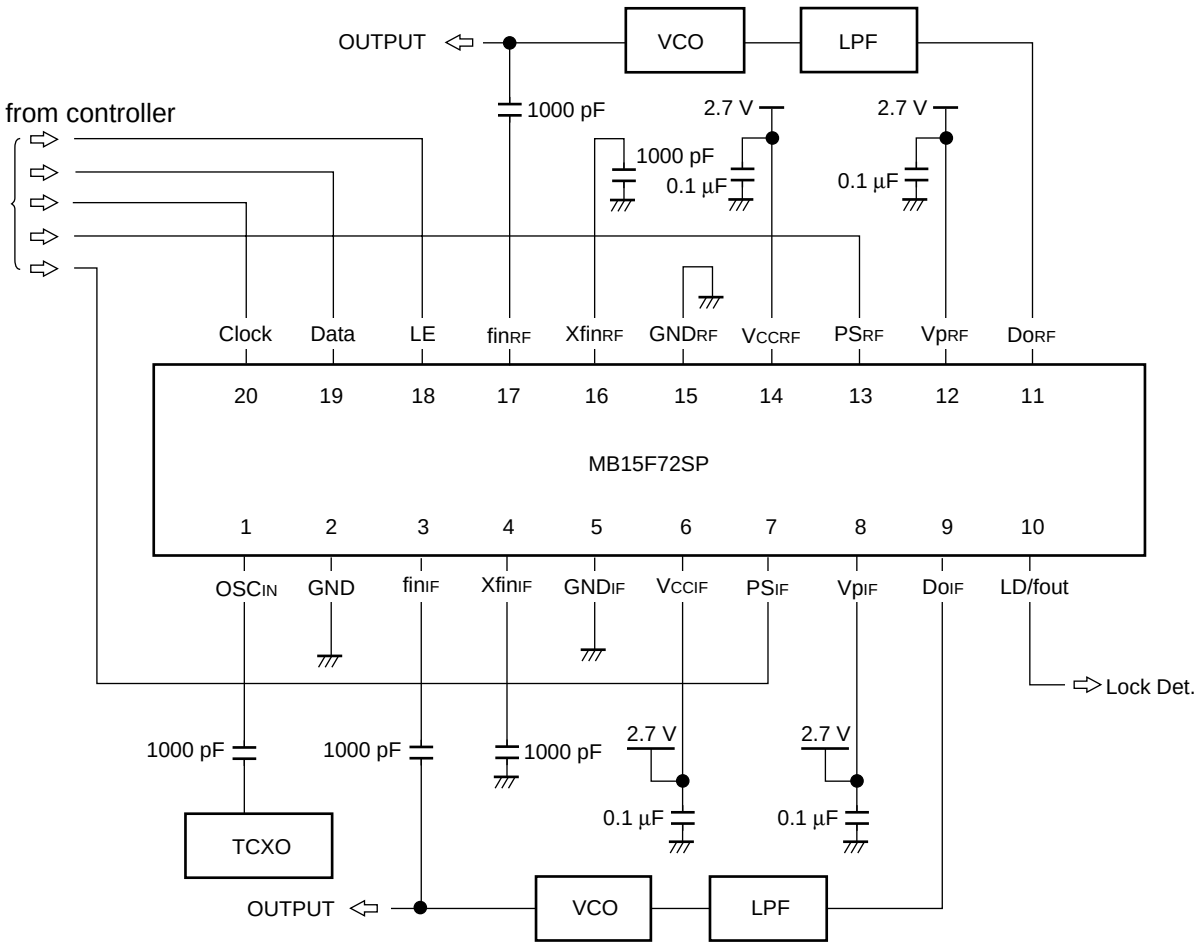
• PLL Lock Up time

755 MHz→680 MHz within ± 1 kHz
Hch→Lch 1.133 ms





■ APPLICATION EXAMPLE



Notes : • Clock, Data, LE : Schmitt trigger circuit is provided(insert a pull-down or pull-up registor to prevent oscillation when open-circuit in the input).
• Terminal number shows that of TSSOP-20.

■ USAGE PRECAUTIONS

(1) V_{CCRF}, V_{PRF}, V_{CCIF} and V_{PIF} must equal equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both V_{CCRF}, V_{PRF}, V_{CCIF} and V_{PIF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

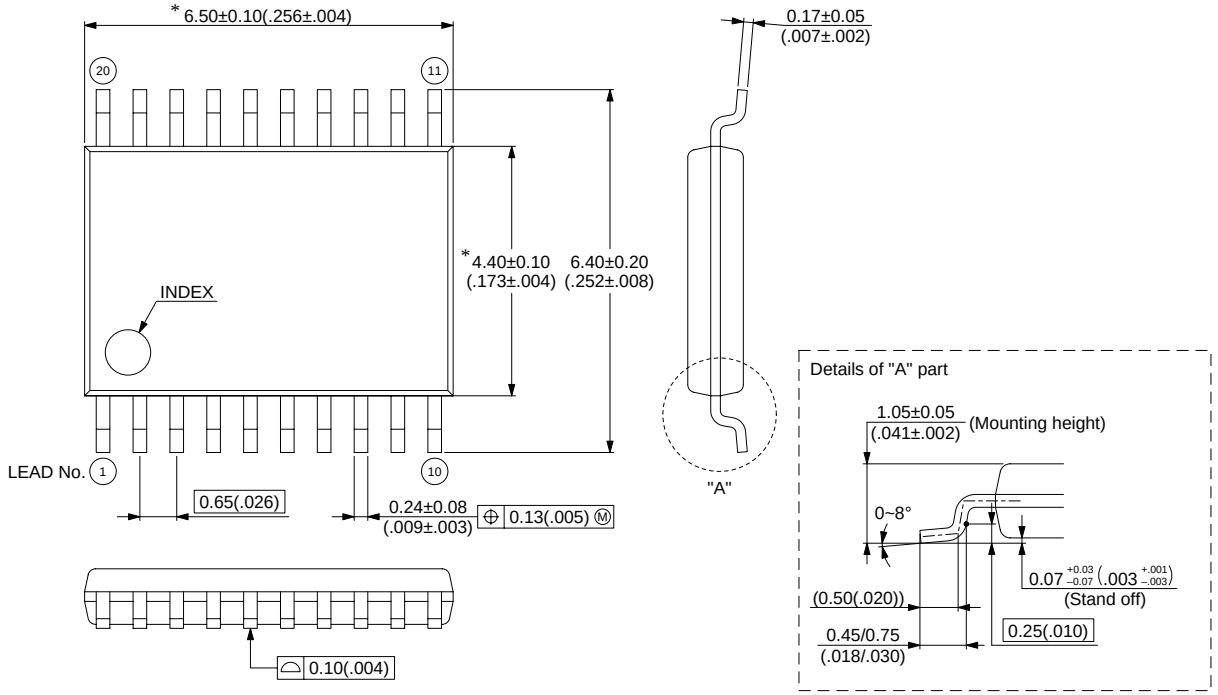
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F72SPPFT	20-pin plastic TSSOP (FPT-20P-M06)	
MB15F72SPPV	20-pad plastic BCC (LCC-20P-M04)	

■ PACKAGE DIMENSIONS

20-pin plastic TSSOP
(FPT-20P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.

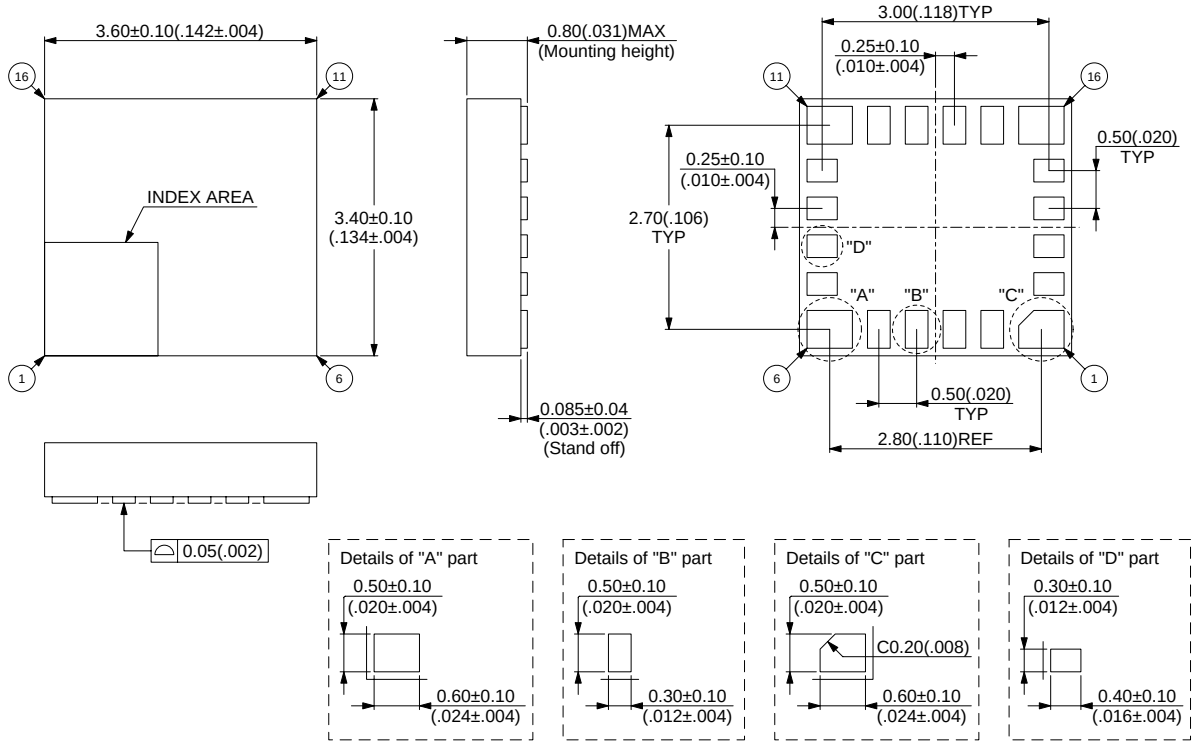


Dimensions in mm (inches)

(Continued)

(Continued)

20-pad plastic BCC
(LCC-20P-M04)



Dimensions in mm (inches)

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