National Semiconductor

May 1991

MM58174A
Microprocessor-Compatible Real-Time Clock

General Description

The MM58174A is a low-threshold metal-gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Timekeeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768 Hz crystal-controlled oscillator.

Features

- Microprocessor compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Independent interrupt system with open drain output
- TTL compatible
- Low power standby operation (2.2V, 10 μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package
- Available for commercial and military temperature ranges

Applications

- Point-of-sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor-controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

Block Diagram

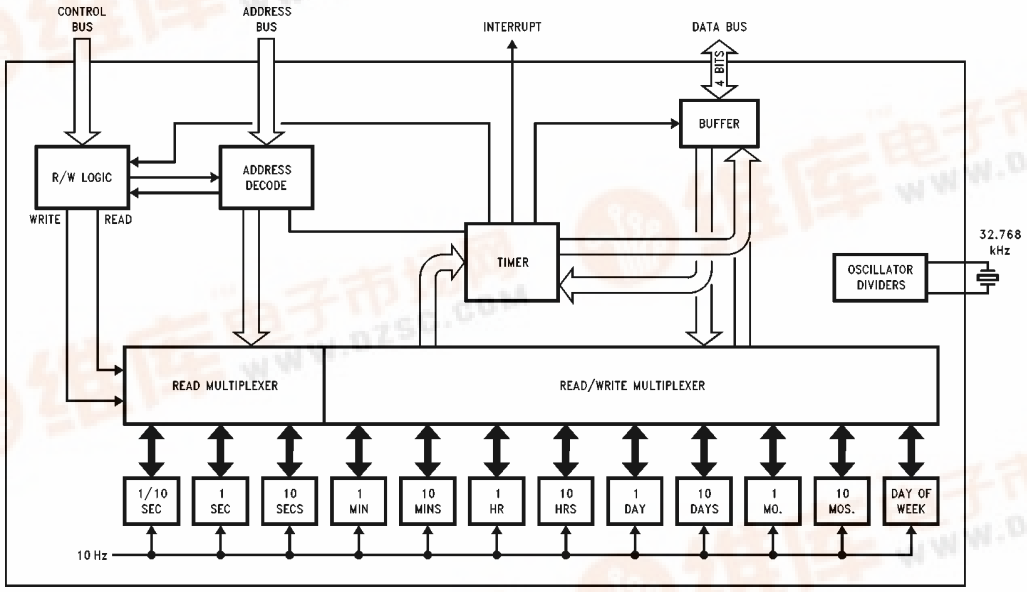

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FIGURE 1

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at All Inputs and Outputs $V_{DD} + 0.3$ to $V_{SS} - 0.3$

Operating Temperature

MM58174AN $-40°C$ to $+85°C$

Storage Temperature $-65°C$ to $+150°C$

$V_{DD}-V_{SS}$ 6.5V

Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{SS} = 0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	Standby Mode (no READ or WRITE Instructions)	2.2		5.5	V
		Operational Mode	4.5		5.5	V
I_{DD}	Supply Current	$V_{DD} = 2.2V$ (Standby)			10	μA
		$V_{DD} = 5V$ (Operating)			1	mA
	Input Logic Levels for Signals: AD0–AD3, DB0–DB3, WR, RD, CS	$V_{DD} = 5V$				
	Logic "1"		2			V
	Logic "0"				0.8	V
	Input Capacitance				10	pF
	Input Current Levels	$V_{DD} = 5V$				
	Current to V_{SS} for Signals: AD0–AD3, DB0–DB3, $\overline{RD}$	$V_{IN} = V_{DD}$			30	μA
	Internal Resistor to V_{DD} for Signals:					
	$\overline{WR}$		30	100		kΩ
	$\overline{CS}$		30	100		kΩ
	Output Logic Levels for Signals:	$V_{DD} = 5V$				
	DB0–DB3					
	Logic "1"	$I_{OH} = -0.1$ mA	2.4			V
	Logic "0"	$I_{OL} = 1.6$ mA			0.4	V
	INTERRUPT (Open Drain)					
	Logic "0"	For $I_{DS} = 1.6$ mA			0.4	V
	Off Leakage	$V_{OUT} = 5V$			5	μA

Functional Description

The MM58174 is a microprocessor bus-oriented real-time clock. The circuit includes addressable real-time counters for tenths of seconds through months and a write only register for leap year calculation. The counters are arranged as bytes of four bits each. When addressed a byte will appear on the data I/O bus so that each word can be accessed independently. If any byte does not contain four bits (e.g., days of the week uses only 3 bits), the unused bits will be unrecognized during a write operation and tied to V_{SS} during a read operation.

The addressable reset latch causes the pre-scaler, tenths of seconds, seconds, and tens of seconds to be held in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code '1111'. The interrupt timer may be programmed for intervals of 0.5 second, 5 seconds, or 60 seconds and may be coded as a single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the internal selected information.

Circuit Description

The block diagram shown in *Figure 1* shows the structure of the CMOS clock chip. A 16-pin DIL package is used.

CRYSTAL OSCILLATOR

This consists of a CMOS inverter/amplifier with on-chip bias resistor and capacitors. A single 6 pF–36 pF trimmer is all that is required to fine tune the crystal (see *Figure 2*). However, for improved stability, some crystals may require a capacitor of typical value 20 pF to be added between pin 14 and ground. The output of the oscillator is blocked by the start/stop F/F.

NON-INTEGER DIVIDER

This counter divides the incoming 32,768 Hz frequency by 15/16 down to 30,720 Hz.

FIXED DIVIDER (512)

This is a standard 9-stage binary ripple counter. Output frequency is 60 Hz. This counter is reset to zero by start/stop F/F.

FIXED DIVIDER (6)

This is a 3-stage Johnson counter with a 10 Hz output signal. This counter is reset to zero state by the start/stop F/F.

SYNCHRONIZATION STAGE

Both 10 Hz and 32,768 Hz clocks are fed into this section. It is used to generate a pulse of 15.25 μs width on the rising edge of each 10 Hz pulse.

This pulse is used to increment all the seconds, minutes, hours, days, months, and year counter and also to set the data changed F/F.

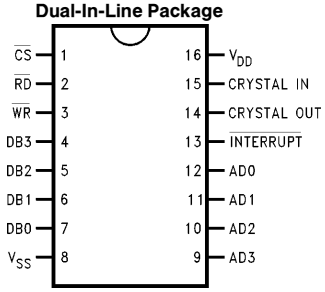
DATA CHANGED F/F

This is set by the rising edge of each 10 Hz pulse to indicate that the clock value has changed since the last read operation. It is reset by any clock read command.

The flip flop sets all data bus bits to a "1" during RD time indicating that a register has been updated. This transient condition may occur at the end of the Read Data strobe. Hence, invalid data may still be read from the clock, if the strobe width was less than 3 μs.

Connection Diagram

Dual-In-Line Package



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Top View
Order Number MM58174AN
See NS Package Number N16A

The possibility may be overcome by implementing a further read of the tenths of seconds register at the end of every series of reads (starting with a read at the tenths of seconds register) and checking for unchanged data.

SECONDS COUNTERS

There are three counters for Seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds

The outputs of all three counters can be separately multiplexed on to the command 4-bit output bus. Table I shows the address decoding for each counter. All three counters are reset to zero by the start/stop F/F.

MINUTES COUNTERS

There are two Minutes counters:

a) units of minutes

b) tens of minutes

Both counters are parallel loaded with data from the 4-bit input bus when addressed by the microprocessor and a Write Data Strobe pulse given. Similarly, the output of both counters can be read separately onto the common 4-bit output bus (Table I).

HOURS COUNTERS

There are two Hours counters which will count in a 24-hour mode:

a) units of hours

b) tens of hours

Both counters have identical parallel load and read multiplex features to the Minutes counters.

SEVEN DAY COUNTER

There is a 7-state counter which increments every 24 hours. It will have identical parallel load and read multiplex capabilities to the Minutes and Hours counters. The counter counts cyclically from 1–7.

Circuit Description (Continued)

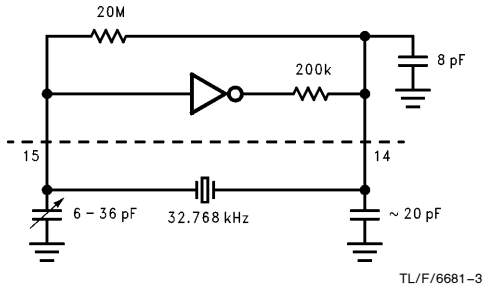


FIGURE 2. Crystal Oscillator

DAYS COUNTER

There are two Days counters:

a) units of days

b) tens of days

The Days counters will count up to 28, 29, 30, or 31 days depending on the state of the Months counters and the Years Status Register. Days counters have parallel load and read multiplex capabilities.

MONTHS COUNTERS

There are two Months counters:

a) units of months

b) tens of months

The Months counters have parallel load and read multiplex capabilities.

YEARS STATUS REGISTER

The Years Status register is a shift register of 4 bits. It will be shifted every year on December 31st. The status register must be set in accordance with Table III. No readout capability is provided.

CHIP SELECT ($\overline{CS}$)

An external chip select is provided. The chip enable is active low.

COUNTER AND REGISTER SELECTION

Table I shows the coding on the address lines AD0–AD3 which select the registers in the circuit to be either parallel loaded or read on to the output bus.

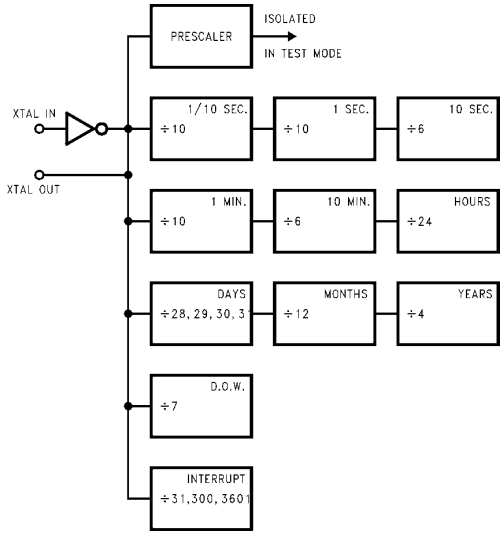


FIGURE 3. Test Mode Organization

START/STOP (RESET) LATCH

A logic ''1'' on DB0 at chip address 14 (E) will start the clock running, a logic ''0'' will stop the clock. This function allows the loading of time data into the clock and its precise starting. The clock starts at 0.1 seconds.

TEST MODE

This mode is incorporated to facilitate production testing of the circuit. In this mode, the 32,768 Hz clock is fed forward as shown in *Figure 3.* For normal operation, the circuit must be set to the non-test mode as part of the system initialization. This is accomplished by writing a logic ''0'' to DB3 at AD0.

TABLE I. Address Decoding for Internal Registers

Selected Counter		Address Bits				Mode
		AD3	AD2	AD1	AD0	
0	Test Only	0	0	0	0	Write Only
1	Tenths of Secs.	0	0	0	1	Read Only
2	Units of Secs.	0	0	1	0	Read Only
3	Tens of Secs.	0	0	1	1	Read Only
4	Units of Mins.	0	1	0	0	Read or Write
5	Tens of Mins.	0	1	0	1	Read or Write
6	Units of Hours	0	1	1	0	Read or Write
7	Tens of Hours	0	1	1	1	Read or Write
8	Units of Days	1	0	0	0	Read or Write
9	Tens of Days	1	0	0	1	Read or Write
10	Day of Week	1	0	1	0	Read or Write
11	Units of Months	1	0	1	1	Read or Write
12	Tens of Months	1	1	0	0	Read or Write
13	Years	1	1	0	1	Write Only
14	Stop/Start	1	1	1	0	Write Only
15	Interrupt	1	1	1	1	Read or Write

Circuit Description (Continued)

TABLE IIa. Interrupt Selection Data

Mode: Address 15, Write Mode				
Function	**DB3**	**DB2**	**DB1**	**DB0**
No Interrupt	X	0	0	0
Int. at 60 Sec. Intervals*	0/1	1	0	0
Int. at 5.0 Sec. Intervals*	0/1	0	1	0
Int. at 0.5 Sec. Intervals*	0/1	0	0	1

*+ 16.6 ms

DB3 = 0, single interrupt

DB3 = 1, repeated interrupt

TABLE IIb. Interrupt Read Back (Status)

Mode: Address 15, Read Mode				
Interrupt Status	**DB3**	**DB2**	**DB1**	**DB0**
Reset	X	0	0	0
60 Sec. Signal	X	1	0	0
5.0 Sec. Signal	X	0	1	0
0.5 Sec. Signal	X	0	0	1

X = don't care state

TABLE III. Years Status Register

Mode: Address 13, Write Mode				
	DB3	**DB2**	**DB1**	**DB0**
Leap Year	1	0	0	0
Leap Year-1	0	1	0	0
Leap Year-2	0	0	1	0
Leap Year-3	0	0	0	1

Note: Leap year counter rolls over on December 31 @ 23:59:59.

INTERRUPT SYSTEM

The interrupt output and its frequency of operation is enabled by writing to address 15 (see Table IIa). To ensure correct operation, the interrupt should be serviced within 16.6 ms.

The interrupt is initialized by writing "0" to address 15 and reading the interrupt, i.e., reading at address 15 three times. Initialization must be performed at power on and also if the interrupt is not serviced correctly within 16.6 ms.

SERVICING THE INTERRUPT

In a typical system the open drain interrupt output is wired to the processor interrupt system. Hence, when the interrupt timer times out, the interrupt output is pulled low and the processor is interrupted.

The processor may then reset the interrupt by utilizing the following procedure:

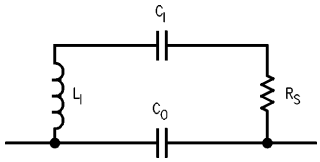
Read Address 15 three times.

This resets the interrupt output and restarts the interrupt timer when in the repeat mode.

It is recommended that the interrupt output is connected to a unique processor port.

CRYSTAL PARAMETERS

Figure 4 is an electrical representation of the crystal along with some typical values. The 32.768 kHz crystal is an NT CUT (tuning fork type) or XY BAR for use in a parallel resonant Pierce oscillator.



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$C_1 \approx 0.003$ pF $R_S \approx 35$ kΩ

$C_0 \approx 3.0$ pF

FIGURE 4. Typical Crystal Parameters

DEVICE INITIALIZATION AND OSCILLATOR SETTING

When first installed or if the battery back-up has failed, the MM58174A will require to be properly initialized. The following sequence is a suggested flow of operations to achieve this.

Action	**Result**
1) Apply power.	Clears interrupt timer chain.
2) Write "0" to address 15.	
3) Read 3 times from address 15.	Clears interrupt output logic.
4) Write "0" on DB3 to address 0.	Clears test mode.
5) Write "0" on DB0 to address 14.	Stops clock running.
6) Set up timekeeping registers.	Load real-time into device time registers, minutes to leap years.
7) Write "1" on DB0 to address 14.	Starts timekeeping synchronized to an external time source.
8) Program and start interrupts.	Commence interrupt timing, if so required.

OSCILLATOR SETTING

Directly connecting a frequency meter to the Crystal Out pin (14) will not allow correct frequency setting because of the extra capacitive loading of the meter. One possibility for setting is to use a high impedance probe or a CMOS buffer to keep the loading as low as possible (e.g., 100 x 2 pF probe). Alternatively, a buffered output of 16.384 kHz OSC/2 can be produced on DB0 by applying the following procedure:

Action	**Result**
1) Write a "1" on DB3 to address 0.	Selects test mode.
2) Write a "1" on DB0 to address 14.	Starts clock timing.
3) Read at address 1 (tenths of secs).	"Data Changed" signal is read.
4) Read at address 1 and HOLD the strobe LOW.	16.384 kHz appears on DB0.
5) Adjust trimmer capacitor.	

There must be no extra activity on the $\overline{RD}$ line between steps 3 and 4 or only the normal "Data Changed" signal will be observed on the data bus. Thus if the normal host processor system is being used to generate the chip waveforms, proper care must be taken.

Timing Waveforms

READ MODE

Figure 6 gives detailed timing for the transfer of data from peripheral to microprocessor. See Table IV.

All times are measured from (or to) valid logic "0" level = 0.8V or valid logic "1" level = 2.0V.

WRITE MODE

Figure 7 gives detailed timing for the transfer of data from microprocessor to peripheral. See Table V.

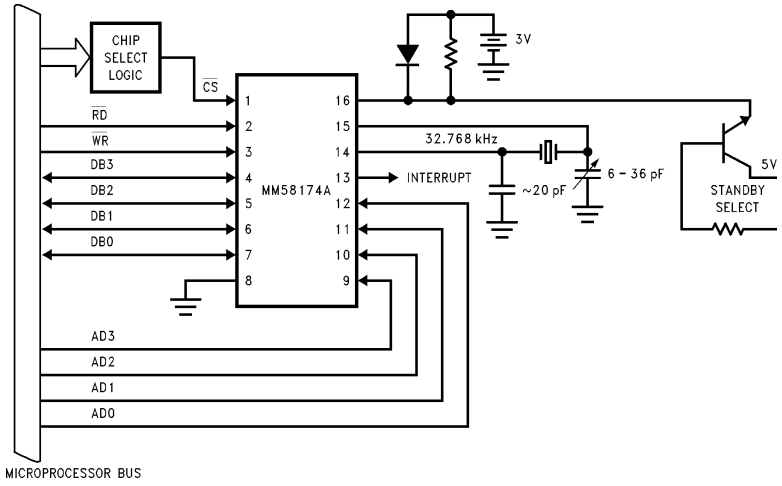

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FIGURE 5. Typical Microprocessor Interface

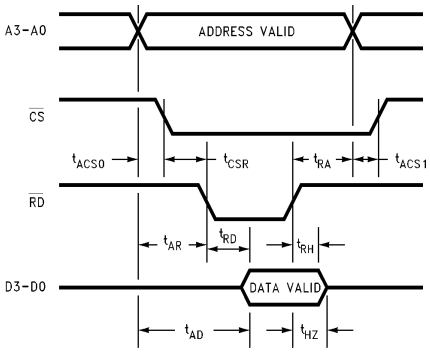

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FIGURE 6. Read Cycle Waveforms

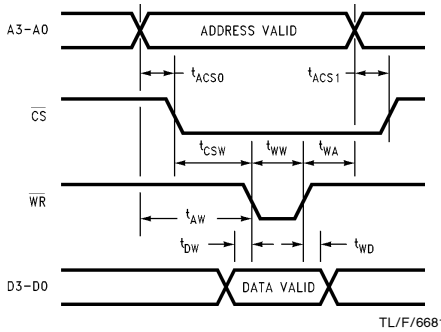

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FIGURE 7. Write Cycle Waveforms

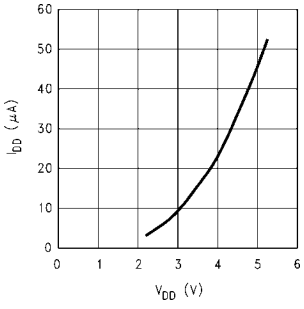

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FIGURE 8. Typical Supply Current vs Supply Voltage during Power Down

Operating Conditions MM58174AN $T_A = -40°C$ to $85°C$, $V_{DD} = 5V$

TABLE IV. Read Timing: Data from Peripheral to Microprocessor

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSR}	Chip Select ON to Read Strobe	0			ns	
t_{RD}	Read Cycle Access Time from Read Strobe to Data Bus Valid		900	450	ns	$C_L = 100$ pF
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	0	330		ns	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	70		500	ns	
t_{ACS1}	Address Change to Chip Select OFF	0		40	ns	
t_{AD}	Address Bus Valid to Data Valid		1850	850	ns	$C_L = 100$ pF
t_{HZ}	Time from Trailing Edge of Read Strobe until Interface Device Bus Drivers are in TRI-STATE® Mode	0	330		ns	
t_{RW}	Read Strobe Width		14		μs	
t_{AR}	Address Bus Valid to Read Strobe	500			ns	

Note 1: In order not to degrade timekeeping accuracy, the number of Read strobes in any one second should be less than 10,000.

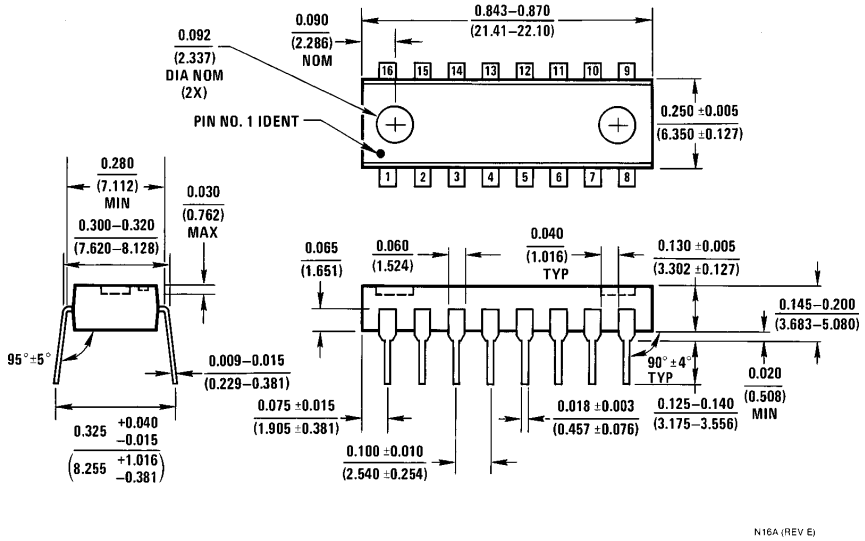
Note 2: If address and read occur simultaneously then they must exist for $t_{AR} + t_{AD}$.

TABLE V. Write Timing: Data from Microprocessor to Peripheral

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSW}	Chip Select ON to Write Strobe	0		450	ns	
t_{AW}	Address Bus Valid to Write Strobe	725			ns	
t_{WW}	Write Strobe Width	670			ns	
t_{DW}	Data Bus Valid before Write Strobe	70			ns	
t_{WA}	Address Bus Hold Time following Write Strobe	165			ns	
t_{WD}	Data Bus Hold Time following Write Strobe	185			ns	
t_{ACS1}	Address Change to Chip Select OFF ($\overline{CS} = 1$)	0			ns	

Note 3: If address and write occur simultaneously, then they must exist for t_{AW} and t_{WW}.

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM58174AN
NS Package Number N16A

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