



## W55FXX

# SERIAL FLASH EEPROM SERIES

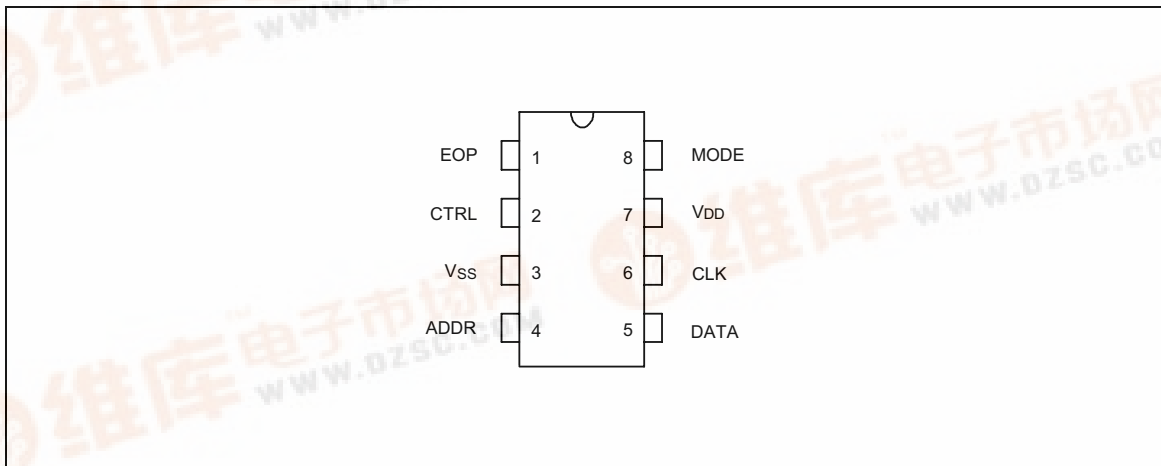
## GENERAL DESCRIPTION

The W55FXX is a serial input/output flash EEPROM series that is typically used as the memory cell of a W51300 (voice recorder controller) or the ROM code emulator for the PowerSpeech™ series. The single voltage supply eliminates the need for an extra pump circuit during programming and erasing.

## FEATURES

- Provides CLK, ADDR, and DATA pins to operate with Winbond PowerSpeech™ series
- 512K/1M/2M memory sizes available
- Directly cascadable for longer duration
- Fast frame-write operation
  - Frame (32 bits) program cycle time: 400  $\mu$ S (typ.)
- Fast whole-chip-erase duration: 50 mS (max.)
- Read data access time: 500 nS (max.)
- Program/erase cycles: 10,000 (typ.)
- Data retention: 10 years (typ.)
- Low power consumption:
  - Operating: 5 mA (typ.)
  - Standby: 2  $\mu$ A (typ.)

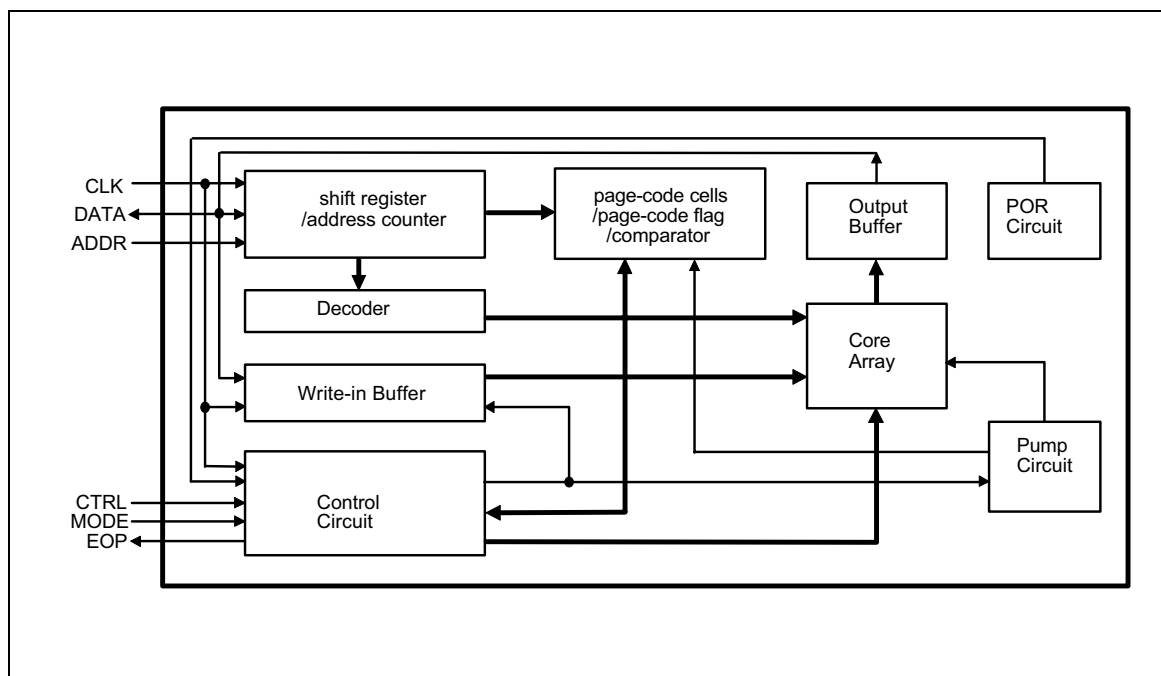
## PIN CONFIGURATION



## PIN DESCRIPTION

| NO. | PIN NAME | I/O | DESCRIPTION                                                                                                |
|-----|----------|-----|------------------------------------------------------------------------------------------------------------|
| 1   | EOP      | O   | End of process signal output                                                                               |
| 2   | CTRL     | I   | Enable signal for program and erase operations when MODE = 0<br>Input clock for mode counter when MODE = 1 |
| 3   | Vss      | I   | Ground                                                                                                     |
| 4   | ADDR     | I   | Input clock for start address shift-in                                                                     |
| 5   | DATA     | I/O | Bidirectional data line                                                                                    |
| 6   | CLK      | I   | Input clock for data write-in and read-out                                                                 |
| 7   | VDD      | I   | Positive voltage supply                                                                                    |
| 8   | MODE     | I   | Mode select control pin                                                                                    |

## BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

| PARAMETER                   | SYMBOL  | CONDITION | RATED VALUE      | UNIT |
|-----------------------------|---------|-----------|------------------|------|
| Operating Temp.             | TOPR    | -         | 0 to +70         | °C   |
| Storage Temp.               | TSTG    | -         | -65 to +150      | °C   |
| Power Supply                | VDD-VSS | -         | -0.3 to +7.0     | V    |
| Input DC Voltage            | VDC     | All pins  | -0.5 to VDD +1.0 | V    |
| Transient Voltage (< 20 nS) | VTRAN   | All pins  | -1.0 to VDD +1.0 | V    |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## DC CHARACTERISTICS

(VDD = 4.5V, VSS = 0V, TA = 25° C)

| PARAMETER                           |       | SYMBOL | CONDITIONS                                      | LIMITS        |      |      | UNIT |
|-------------------------------------|-------|--------|-------------------------------------------------|---------------|------|------|------|
|                                     |       |        |                                                 | MIN.          | TYP. | MAX. |      |
| Operating voltage                   |       | VDD    | -                                               | 2.4<br>(Note) | 4.5  | 5.5  | V    |
| Standby current                     |       | ISB    | All inputs = GND<br>DATA & EOP open             | -             | 2    | 4    | μA   |
| Operating current                   |       | IOP    | In read mode<br>DATA & EOP open<br>FOSC = 1 MHz | -             | 5    | 10   | mA   |
| Input voltage                       | High  | VIH    | All input pins                                  | 2.0           |      | VDD  | V    |
|                                     | Low   | VIL    |                                                 | -0.3          | -    | 0.8  | V    |
| Output current                      | Sink  | IOL    | VOL = 0.5V                                      | 2.5           | 5    | -    | mA   |
|                                     | Drive | IOH    | VOH = 4.0V                                      | -2.5          | -5   | -    | mA   |
| Input leakage current of CTRL, MODE |       | ILI1   | VIN = 4.5V                                      | -             | -    | 4.5  | μA   |
| Input leakage current of DATA       |       | ILI2   | VIN = 0V                                        | -             | -    | -4.5 | μA   |

Note: For been working with W52900, the minimum operating voltage couldn't be less than 3.6 volt.

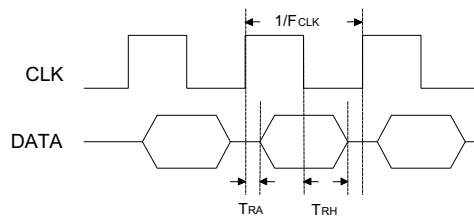
## AC CHARACTERISTICS

(V<sub>DD</sub> = 4.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 25° C)

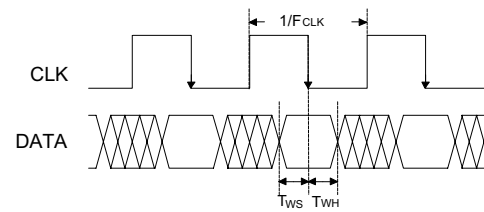
| PARAMETER                                               | SYMBOL | CONDITIONS            | MIN. | TYP. | MAX. | UNIT |
|---------------------------------------------------------|--------|-----------------------|------|------|------|------|
| MODE pulse width                                        | TMP    | -                     | 1    | -    | -    | μS   |
| CTRL pulse width                                        | TWP    | Page coding mode      | 400  | -    | 700  | μS   |
| Clock frequency of ADDR                                 | FADDR  | -                     | -    | -    | 1    | MHz  |
| Clock frequency of CLK                                  | FCLK   | -                     | -    | -    | 1    | MHz  |
| Clock frequency of CTRL                                 | FCTRL  | -                     | -    | -    | 1    | MHz  |
| Interval between ADDR end & CLK begin                   | Ti     | Read/Write mode       | 1    | -    | -    | μS   |
| Interval between CLK & CTRL                             | TGCC   | Write mode            | 1    | -    | -    | μS   |
| Interval between ADDR & CTRL                            | TGCA   | Page coding mode      | 1    | -    | -    | μS   |
| Interval between addressing end & block-erase begin     | TAE    | Block erase mode      | 1    | -    | -    | μS   |
| Interval between MODE rising edge & CTRL clock begin    | TMB    | Mode selection        | 500  | -    | -    | nS   |
| Interval between CTRL clock end & MODE falling edge     | TME    | Mode selection        | 500  | -    | -    | nS   |
| Interval between MODE falling edge & another pin active | TGM    | -                     | 1    | -    | -    | μS   |
| Data access time                                        | TRA    | Read mode             | -    | -    | 500  | nS   |
| Data set up time                                        | TWS    | Write mode            | 250  | -    | -    | nS   |
|                                                         | TAS    | -                     | 250  | -    | -    | nS   |
| Data hold time                                          | TRH    | Read mode             | 0    | -    | -    | nS   |
|                                                         | TWH    | Write mode            | 10   | -    | -    | nS   |
|                                                         | TAH    | -                     | 10   | -    | -    | nS   |
| Programming duration                                    | TPR    | Write mode            | 400  | -    | -    | μS   |
| Whole-chip-erase time                                   | TWE    | Whole-chip-erase mode | 45   | -    | 50   | mS   |
| Block-erase time                                        | TBE    | Block-erase mode      | 40   | -    | 45   | mS   |

## TIMING WAVEFORM

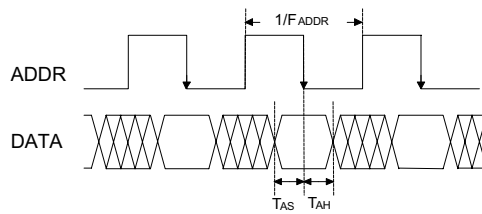
Read Cycle



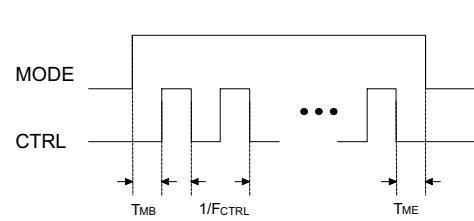
Write Cycle



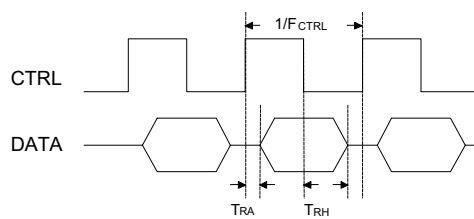
Address Shift-in Cycle



Mode Select Duration

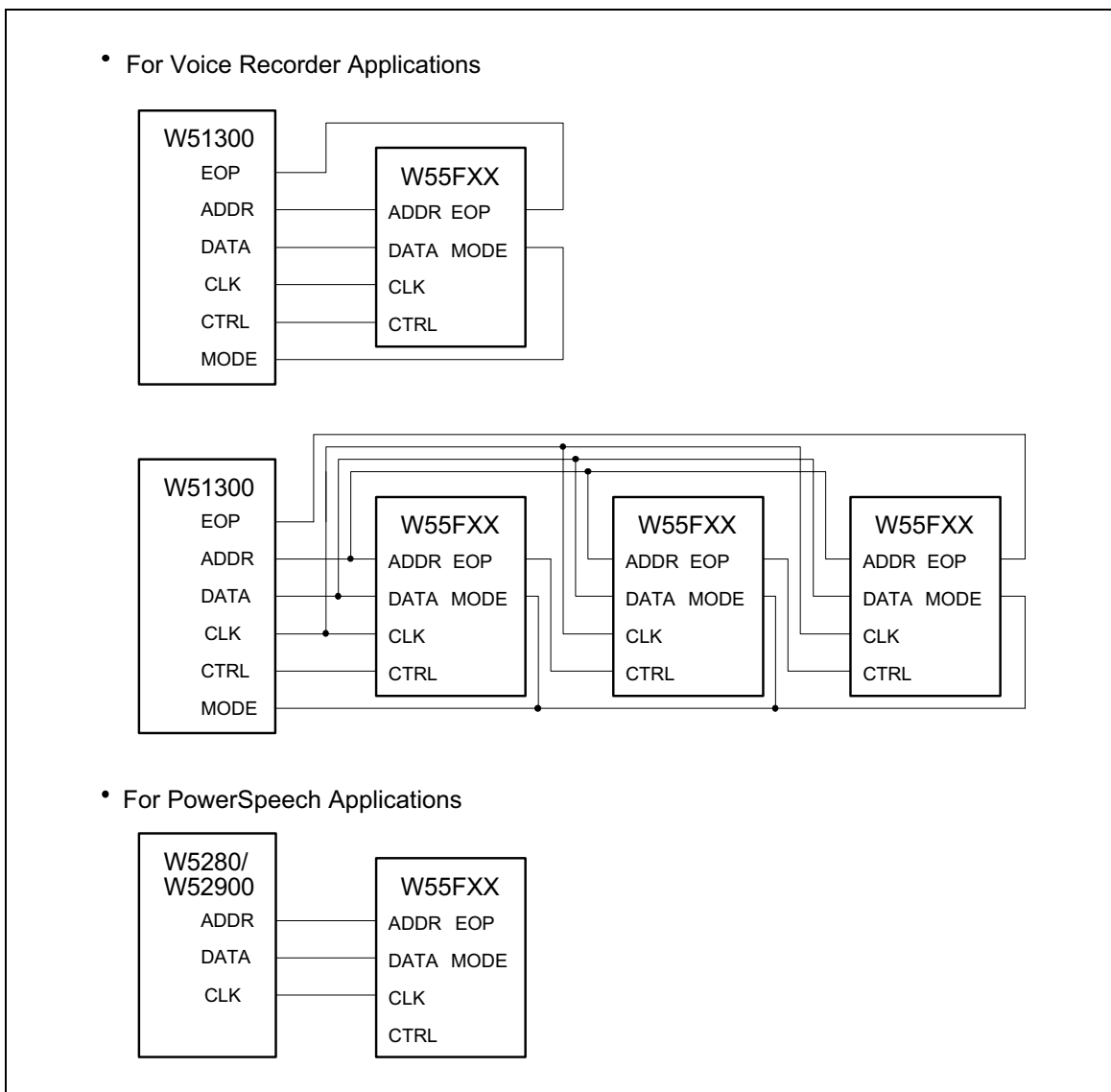


Page-code Cell Read Out Cycle



Note: The duty cycle of any clock is 50%.

## APPLICATION CIRCUITS (for reference only)



## ORDERING INFORMATION

| PART NO. | MEMORY SIZE |
|----------|-------------|
| W55F05   | 512K BITS   |
| W55F10   | 1M BITS     |
| W55F20   | 2M BITS     |



**W55FXX**



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Note: All data and specifications are subject to change without notice.